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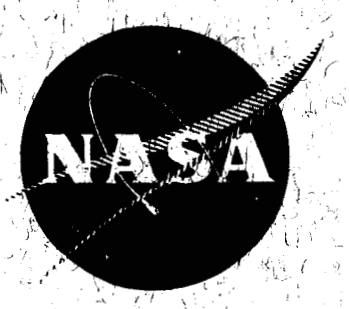

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DEVELOPMENT OF A 1.6-KW, 2000-VOLT, HIGH-FREQUENCY DC-DC CONVERTER FOR ION THRUSTORS USING A MODULAR DESIGN AND AN INDUCTIVE ENERGY PUMPING TECHNIQUE FOR CONVERSION, REGULATION AND PROTECTION

by

Edward T. Moore, Thomas G. Wilson, and Joseph N. McIntire

prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

CONTRACT NAS 3-6264

Wilmore Electronics Company, Inc.

Box 2973 West Durham Station, Durham, North Carolina 27705

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SUMMARY REPORT

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December 8, 1965

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ABSTRACT

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Primary objectives in the design of this modular converter were very low weight, high efficiency, and a ruggedness and general compatibility with the transient-inducing nature of the ion-engine load. High-frequency silicon power transistors were used with current-feedback base drive at a switching frequency of 10 kc. The use of special energy-storage power transformers was found to make possible a very efficient, lightweight, nondissipatively regulated converter which is physically very simple. These special transformers play an integral role in the voltage conversion, filtering, regulation, and protection functions which take place in the converter.

Author

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SUMMARY

The two primary objectives of this research and development contract were (1) to investigate the application of certain unconventional circuit techniques to a high-voltage converter for use with ion engines and (2) by using these circuit techniques, to design and construct an Experimental Model of an efficient, lightweight converter. A modular approach was employed in the design of the Experimental Model which provides a nondissipatively regulated d-c output of 1600 watts at 2000 volts. Six identical building-block stages are used in the modular configuration; the converter input voltage is 25-31 volts d-c.

Central to the design of the converter is the use of two energy-storage transformers per building-block stage. These special transformers involve multiple windings and a magnetic path containing a small air gap. Each cycle of the operation of the converter involves a half cycle during which inductive energy is stored in these transformers and a half cycle during which this stored energy is delivered to the load. Base drive to the high-frequency silicon power transistors is by means of a current-feedback arrangement involving small saturable current transformers. A maximum switching frequency of 10 kc is employed; the nondissipative regulation scheme involves varying this frequency to compensate for changes in input voltage or load.

The Experimental Model exhibits an efficiency which is nearly constant with variations in input voltage and which varies from 67% at 5% of full load to 88.8% at 64% of full load, dropping to 86.5% at 100% of full load. The total weight of the components of the 1.6 KW Experimental Model is 16.4 pounds or 10.25 pounds per kilowatt. An especially interesting feature of this converter, predicted during the design and verified by the Experimental Model, is that short circuiting the 2000-volt output produces no current surges through either the output rectifiers or the power transistors.

As a result of this work it has been demonstrated that the energy-

storage transformer approach is well suited for use in lightweight non-dissipatively regulated, high-voltage d-c to d-c converters for ion-engines. The particular current-feedback base drive and regulation scheme which was developed makes possible a modular configuration having a high degree of physical simplicity.

Based on the data obtained and experience to date, it is felt that improvements can be made in both the weight and efficiency of the present converter. These improvements would involve certain changes in the design of the energy-storage transformers and would require the usage of a higher input voltage such as 56 volts.

I. INTRODUCTION

A reaction-driven space vehicle receives its thrust by accelerating and expelling propellant mass. One very important criteria for such propulsion systems is the velocity to which propellant mass may be accelerated and expelled, since this determines the total mass of propellant necessary to accomplish a particular mission.[1]* In the case of chemical rockets and nuclear rockets in which the propellant is energized by a thermal heating process, the exhaust velocity is limited by the temperature capability of the chemical reaction or of the confining walls. Nonthermal (electric) acceleration systems, however, are not subject to these constraints, and a considerable amount of effort is therefore being devoted to the development of electric thrustors.

The weight, efficiency, and reliability of the power-conditioning system which is used with an ion-engine will, of course, be factors which directly affect the degree to which the ion engine realizes its theoretical advantages. Certain of the requirements which need to be met by such a power-conditioning system are discussed in Reference 2; other requirements are presently becoming more adequately defined as engine development and testing progresses. One particular problem is the transient-inducing nature of the ion-engine as an electrical load on a high-voltage power supply. This tendency toward frequent and severe electrical breakdown (arcing) requires a high degree of ruggedness in the power supply and makes the attainment of a very lightweight supply more difficult. Much less research and development work has been done in the high-power, high-voltage area than in other areas of power-conditioning technology. (2-5)

This contract involved the development of a modular d-c to d-c converter for ion-engine applications. There were two main objectives:

(1) To explore and evaluate the usefulness of certain unconventional power conversion techniques involving the use of special energy-storage transformers.

(2) To provide to NASA an Experimental Model of a lightweight and efficient 2000-volt, 0.8-ampere d-c to d-c converter by using these techniques in a modular approach.

The resulting Experimental Model exhibits excellent performance characteristics and a high power-to-weight ratio. It also demonstrates the feasibility of building a highly efficient high-power converter for an operating frequency of 10 kc with presently available transistors and magnetic materials. In addition to verifying the usefulness of the original design proposals, such as the energy-storage-transformer technique, it is felt that the results of this contract indicate that the use of a modular approach has considerable advantages in power-conditioning systems for ion engines and should receive further attention.

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5. NASA Contract No. NAS 3-5917, Westinghouse Electric Corporation, concerning a program similar to that of Reference 4 in which gate controlled switches (GCS) rather than transistors were used as the power switching elements.

II. OBJECTIVES AND BASIC SYSTEM DECISIONS

The main electrical design objectives for this dc-to-dc converter were as follows:

(a) Input: 28 volts, ± 10%

(b) Nominal output: 2000 volts, 0-0.8 amperes, direct current

(c) Regulation of the output voltage from 30% of full load to full load: ± 5%

(d) Output voltage regulation not to exceed + 10% at no load

(e) RMS ripple current from the source not to exceed 2% of the average source current at full load

(f) RMS ripple in the output voltage not to exceed 5% where percent ripple in the output voltage is defined as (RMS ripple) x (100)/(2000)

Central to the design of this converter is the use of the energy-storage-transformer approach and current-feedback base drive for the power transistors. A primary design objective was the development of a converter using these techniques which, although highly rugged and quite able to withstand the transient-inducing characteristics of an ion-engine load, nevertheless is characterized by a very light weight.

Certain special characteristics were desired. One of these was the need for soft turn on of the converter output voltage and means for adjusting this soft turn on, or rate of rise of the output voltage, over a wide range. Another was the desire for an adjustable "blink-off time". The term "blink-off time" as used in this report refers to the time period during which the converter remains off before returning soft on after its protection system has been actuated by an overload or short circuit.

An early system decision was the use of a modular approach to the design of this 1600-watt converter. The decision to use six rather than some other number of building-block stages was made primarily on the basis of two factors: (1) the use of six stages for this converter resulted in a per-stage power level which made possible near-optimum usage of the high-frequency power transistors and rectifiers selected for use in the converter, and (2) six was the least number of stages which would readily allow the converter to be designed such that, in the event of failure of one stage, the remaining stages of the converter would have the capability to provide full output power and voltage. The use of a lesser number of stages requires that each stage have a correspondingly greater reserve power and voltage capability. For example, if only two stages are used and it is desired that either stage be able to supply the full output voltage and power

then this requirement will cause the weight of the converter to be nearly doubled. With six stages, however, only a 20% per-stage reserve capability is necessary in order to be able to provide full output in the absence of one stage.

Primarily because of the advantage of being able to operate at a considerably higher base-plate temperature and because of a generally lesser susceptibility to high-energy electrical transients on the part of silicon semiconductors, only silicon semiconductors were used in the design of this converter. All capacitors and other thermally vulnerable components are high temperature types (except for the capacitors of the converter input filter for which computer grade electrolytics were used in the Experimental Model because of price considerations). A design objective was to select components and provide an electrical design such that this converter could, if packaged for flight use, be operated reliably at a base plate temperature of 90°C.

Since weight reduction was a primary design goal, it was necessary that the converter employ a high switching frequency. Primarily from a consideration of losses in the magnetic components rather than limitations of available high-speed switching transistors, a frequency of 10 kc/s was selected.

Because of temperature limitations and low saturation flux level, the use of ferrite for the power transformers was excluded from consideration. Supermendur, a vanadium-cobalt-iron alloy, has recently been made commercially available both in the form of cut C cores and closed tape-wound cores. Cut C cores of this material were initially considered for the energy-storage power transformers of this converter. They were, however, found to be unavailable in 1-mil material. Additionally, because of its much lower resistivity (26 vs. 50 microhm-cm.) the losses of Supermendur tend to increase much more rapidly with frequency than those of 3% silicon-iron alloys. On the basis of relative weights and losses, cut C cores of 1-mil grain oriented silicon-iron were considered to be best suited for this lightweight 10-kc converter and were therefore used in the Experimental Model.

Efficiency requirements dictated the use of power transistors with an exceptionally high switching speed and low saturation resistance. Several transistor manufacturers are now marketing double-diffused and triple-diffused silicon power transistors which have switching speeds that are quite attractive for a high-frequency converter of this type. At the time work was initiated on this contract, however, there were no suitable high-speed devices available with voltage ratings significantly above 100 volts. The power transistor which was finally selected for use in the Experimental Model, the planar triple-diffused Honeywell (now Solitron) type MHT8302, has a rated breakdown voltage (BV_{CBO}) of 100 volts. This is a 30-ampere device and proved to be quite satisfactory at the 28-volt input voltage level of the Experimental Model.

In the energy-storage-transformer approach being used, the power transistors are cyclically required to block a direct voltage which is equal to approximately twice the input voltage to the converter. In view of the voltage ratings of the high-frequency power transistors which were available at the start of work under this contract an input voltage of 28 volts d-c was selected for the design of the Experimental Model. More recently, however, suitable transistors with considerably higher voltage ratings have been made available, and it would appear that a considerable advantage could be gained by using an input voltage level of 56 volts rather than the present 28 volts. This possibility is discussed in more detail in Section V of this report.

III. CIRCUIT DESCRIPTION

Since many of the characteristics of this converter result directly from the special nature of the energy-storage transformers, these transformers and the principles involved in their use in a nondissipatively regulated d-c to d-c converter are initially reviewed. The basic configuration of the six-stage modular approach used in this converter is described in terms of a block diagram. Schematics of each of the individual subcircuits are then presented along with brief technical descriptions of their design and operation. Finally, attention is directed to a full schematic of the complete six-stage converter and an associated components list.

ENERGY-STORAGE-TRANSFORMER CONVERSION PRINCIPLES

Certain principles which are fundamental to this d-c to d-c converter are best illustrated by a consideration of Figures III-1 and III-2. Core T1 of Figure III-1 has linear characteristics such as shown in Figure III-2, i.e. an increase in flux ($\emptyset$) in core T1 necessarily involves an approximately proportional increase in the ampere turns of magnetomotive force (mmf) applied to the core. Such characteristics are readily obtained by inserting a small air-gap in a high permeability magnetic core. Core T1 and its windings will be referred to as an "energy-storage transformer" in much of the discussion to follow. The circuit of Figure III-1 functions as a d-c to d-c converter by making use of the fact that an increment of inductive energy may be stored in T1 and its windings on one half cycle through winding N1 and then delivered from this energy-storage transformer to capacitor C_o and the load through winding N2 on the next half cycle.

Voltage Conversion

Assume that, by a drive circuit not shown, transistor Q1 in Figure III-1 is cyclically turned on and off. While transistor Q1 is turned on, the voltage E_{in} is impressed across winding N1 and the flux level in core T1 is increased. The relative winding polarities of windings N1 and N2 are such that the voltage E_{in} impressed across N1 induces a voltage in winding N2 of such polarity that diode D_o is subjected to a reverse voltage and no current is allowed to flow in winding N2. Thus, during the conducting interval of Q1 no energy is delivered to the load but the flux level in core T1 and the magnetomotive force on the core are increased, i.e. energy is stored within T1 and its windings. Then transistor Q1 is turned off for a half cycle. The mmf existing on core T1, of course, cannot be discontinuous. Therefore, when the current through winding N1 is suddenly interrupted by the turning off of Q1, the inductive energy stored in the transformer causes the polarities of the voltages appearing across windings N1 and N2 suddenly to reverse and continuity of mmf is sustained because of the current which then flows through winding N2 and diode D_o into capacitor C_o and the load.

A typical one-cycle flux-versus-mmf path for core T1 is shown by points A, B, C, D in Figure III-2. The flux and mmf increase from point A to point

B as transistor Q1 conducts and decrease from point C to point D during the interval in which Q1 is turned off and energy is discharged through winding N2. The corresponding cyclic currents through transistor Q1 and diode D_o are shown in Figure III-3. The filter capacitor C_o provides a low-ripple voltage E_o to the load.

Regulation

Within the time interval Δt_1 during which transistor Q1 conducts, the change in flux $\Delta\phi_1$ which takes place in core T1 is given by the relation

(1) $E_{in} = N1 \frac{\Delta\phi_1}{\Delta t_1}$ where N1 and E_{in} refer to Figure III-1.

When transistor Q1 turns off, current must flow through winding N2. In order that this current can flow, the voltage in winding N2 must assume the value of the output voltage E_o (plus the drop across diode D_o which will be assumed to be negligibly small compared to E_o). Depending on the value of the load current, the current through winding N2 may either (1) flow during the entire interval Δt_2 that Q1 is turned off, in which case the operating point on the characteristic of core T1 follows a minor loop similar to that shown in Figure III-2 or (2) flow only during the initial part of the interval Δt_2 that Q1 is turned off, in which case a minor loop is followed which includes the residual flux point ϕ_r of core T1. The latter situation, of course, occurs at light loads, whereas the former occurs at heavier loads.

If the load current is large enough that the minor loop does not include the residual-flux point, the flux change $\Delta\phi_2$ which takes place during the interval Δt_2 that Q1 is turned off is given by the relation

(2) $E_o = N_2 \frac{\Delta\phi_2}{\Delta t_2}$

If steady-state conditions exist, $\Delta\phi_2$ must be equal and opposite to $\Delta\phi_1$ as given by Equation (1); otherwise the average flux level in core T1 would increase or decrease by the increment $(\Delta\phi_1 - \Delta\phi_2)$ each cycle. (Such an increase or decrease in the average flux and, therefore, the average mmf existing on core T1 would imply a corresponding increase or decrease in the average current supplied to capacitor C_o and the load, and the load voltage E_o would thereby be increased or decreased so as to again make $\Delta\phi_2 = \Delta\phi_1$.)

Letting $\Delta\phi_2 = \Delta\phi_1$, it is readily shown from equations (1) and (2) that, under steady-state conditions, the output voltage E_o is simply

(3) $E_o = \frac{N_2}{N_1} \frac{\Delta t_1}{\Delta t_2} E_{in}$.

Equation (3) points out the fact that, above some minimum value of load current, the converter output voltage E_o is directly proportional to the ratio of the cyclic conducting time Δt_1 nonconducting time Δt_2 of the power transistor.

As will be explained in more detail in following sections, the converter developed under this contract is characterized by a constant "on" time Δt_1 for its power transistor(s) and it is the "off" time Δt_2 which is varied so as to control the output voltage.

If the load current is so small that the minor operating loop for core T1 includes the residual point ϕ_r, a flux change occurs in winding N2 during only part of the interval Δt_2 and Equations (2) and (3) no longer hold true. The factors affecting the output voltage under these conditions are pointed out below.

In the particular converter developed under this contract, the conducting time Δt_1 of the power transistors is constant whereas the off time Δt_2 is varied to regulate the output voltage. Therefore, under any condition of output load current equal to or less than that load current at which the operating minor loop for core T1 first begins to include the residual flux point ϕ_r, each conducting interval of the power transistor Q1 in Figure III-1 will cause a predetermined minimum amount of energy $U(E_{in})$ to be stored in core T1 and its windings. That is, the operating loop cannot move any further down the characteristic of core T1. This energy is written as $U(E_{in})$ to reflect the fact that it is a function of E_{in}, i. e. it will increase or decrease if E_{in} increases or decreases. Thus, with a predetermined increment of energy $U(E_{in})$ being transferred from the source to the filter capacitor and load each cycle, the frequency f must be made proportional to the output power in order to maintain regulation. This may be expressed as

(4) $U(E_{in})f = E_o I_o$ where U = energy transferred per cycle
f = frequency, cycles per second
E_o = output voltage
I_o = output current

Whether the converter is operating under load conditions under which Equation (3) applies or under load conditions under which Equation (4) applies, it is apparent that controlling the "off" time Δt_2 of the power transistor Q1 is a simple and effective way of nondissipatively controlling the output voltage of the converter.

Protection Characteristics

Through cyclically storing energy introduced on one half cycle through winding N1 and then delivering this energy to the load through winding N2 on the next half cycle, the circuit of Figure III-1 functions as a d-c to d-c voltage converter. A major difference between this method of voltage conversion and more conventional methods is that the extraction of energy from the source and the delivery of energy to the filter capacitor and load occur on opposite half cycles. This fact has considerable significance insofar as protecting transistor Q1 and diode D_o from current transients caused by load short circuits is concerned.

Assume, for example, that the circuit of Figure III-1 (plus, of course, the necessary drive circuit for Q1 which is not shown) is functioning normally with

waveshapes of current through the semiconductor elements as shown in Figure III-4 and that at some time t_1 the load is suddenly short circuited. Whatever energy exists in the filter capacitor C_o is quickly discharged into the short circuit and the output voltage E_o abruptly becomes essentially zero. However, there is no sudden current transient in diode D_o as a result of the load fault condition and no current transient in transistor Q1. What does happen is that, according to Equation (2) which has been previously discussed, the flux change $\Delta\phi_2$ which occurs during the nonconducting half cycle of Q1 becomes very small because the output voltage E_o has become very small. Thus, $\Delta\phi_2$ becomes quite small, while $\Delta\phi_1$ (change in flux while Q1 conducts) remains unchanged. Since $\Delta\phi_2$ no longer can be equal and opposite to $\Delta\phi_1$ the average flux level and the average mmf existing on core T1 begin to cyclically increase.

The behaviors of the currents through transistor Q1 and through diode D_o after a load short circuit which occurs at some time t_1 are shown in Figure III-4. Note that the short circuit at time t_1 produces no sudden current transients in either of the two power-handling semiconductor components but, instead, only a steady rise in the mmf being applied to core T1. At a predictable time t_2 after the short circuit, core T1 will become saturated (unless the fault condition clears itself or is cleared), and at time t_2 the current through transistor Q1 will become quite large and probably damaging to this transistor. Thus, a short circuit can be expected to cause no destructive currents through the semiconductors for a predictable interval of time (t_1 to t_2), and protective measures must be put into effect before time t_2. The interval of time from t_1 to t_2 is a design parameter which can be chosen in accordance with particular system requirements. Thus, this "energy-pumping" manner of d-c to d-c conversion has distinct advantages insofar as protecting the power-handling semiconductor components from load-induced transients is concerned. These advantages result primarily from the fact that in this converter the taking of energy from the source and the delivery of this energy to the load occur on opposite half cycles.

Full-Wave Configuration

The basic power circuit of Figure III-1, although it illustrates certain useful principles, has some significant disadvantages insofar as use, in this simplest form, in an ion thruster would be concerned.

A primary disadvantage of the unsymmetrical configuration of Figure III-1 is that it takes current from the source E_{in} in half-wave pulses and also supplies current to filter capacitor C_o in half-wave pulses. For certain sources, e.g. solar cells, this would be a disadvantage since considerable input-current filtering would be required. Also the size of capacitor C_o for a given ripple in the output voltage would be undesirably large. Perhaps a more serious consequence is the fact that the conversion efficiency would be adversely affected by the losses caused by the relatively large alternating currents which would flow through the effective series resistance of the input and output filter capacitors.

By using two complementary basic conversion circuits of the type shown in Figure III-1, the ripple in the current drawn from the source and the ripple in the output voltage for a given value for filter capacitor C_o can be substantially reduced. Such a full-wave circuit is illustrated in Figure III-5. Note that transformer T1 and transformer T2 are separate, independent transformers; the circuit of Figure III-5 is not analogous in its operation to the widely used conventional parallel inverter configuration. As, for example, transistor Q1 conducts and energy is supplied to winding N1 of core T_1, a reverse voltage is applied to diode D1 by winding N2. Simultaneously, diode D2 conducts and energy stored in core T2 and its windings during the previous half cycle is supplied from winding N4 to capacitor C_o. That is, as energy from the source is stored in transformer T1, energy which has previously been stored is delivered to the load by transformer T2, and vice versa. Depending on the duty cycle of Q1 and Q2, current is drawn from the source for essentially the entire duration of each half cycle and, although there is some ripple component to the current drawn from the source by the full-wave circuit of Figure III-5, the magnitude of this ripple component relative to the average current drawn from the source is much less than is the case for the circuit of Figure III-1. Depending on the characteristics of the source, further reduction in the ripple component of the source current through appropriate filtering may or may not be desirable.

BLOCK DIAGRAM OF THE COMPLETE MODULAR CONVERTER

Figure III-6 shows the basic configuration of the complete converter in block diagram form. Each of the constituent subcircuits will be individually discussed in a later section. The block diagram of Figure III-6, however, serves to focus attention on the modular nature of the design of this high-power converter and to illustrate the basic design approach.

In addition to the six building-block CONVERTER STAGES themselves, the closed-loop regulation system of the inverter involves a voltage divider R1 and R2, a ZENER DIODE REFERENCE VOLTAGE, a DIFFERENTIAL AMPLIFIER which compares the voltage from the voltage divider to the reference voltage, and a VOLTAGE TO PULSE-FREQUENCY CONVERTER which generates pulses having a frequency which is proportional to the "error-signal" output of the differential amplifier. These pulses are fed to the FLIP-FLOP which switches states at a rate determined by the pulse frequency. As will be explained later in more detail, the frequency with which the FLIP-FLOP reverses states is the means whereby the output voltage of the six current-feedback converter stages is controlled.

DESCRIPTION OF THE BUILDING-BLOCK CONVERTER STAGE

Figure III-7 shows the circuit of one of the six identical full wave energy-storage-transformer converters used in the modular Experimental Model. The basic general principles of its operation have been reviewed in preceding pages.

A current-feedback base-drive system is employed in this converter. This method of base drive, in which the base current of each power transistor is pro-

portional on an instantaneous basis to its collector current, is quite advantageous from an efficiency viewpoint. [4, 6] Current feedback also has advantages insofar as some types of overloads are concerned since the power-transistor base current increases with any increase in collector current and the power transistors tend to remain in a saturated condition, i. e. a low-dissipation condition, unless the collector current is allowed to reach extreme values. The particular current-feedback base-drive system developed under this contract provides an efficient and physically very simple means for controlling the duty cycle of each power transistor from a 50% average cyclic conduction time to a zero % average cyclic conduction time in order to nondissipatively regulate the converter output voltage. Because the duty cycle of the power transistors can be reduced all the way to zero by this system, it is well suited for use in a d-c to d-c converter such as this in which it is desired that regulation be maintained from full load all the way to zero load without the necessity for providing a minimum internal load.

In Figure III-7, transformers T1 and T2 are the power transformers, i. e. the "energy-storage" transformers. Transistors Q1 and Q2 are the power-handling switching transistors. Transformers T3 and T4 are small, saturable current transformers. Transistors Q3 and Q4 are used to cause proper resetting of T3 and T4 after each conduction interval of the main power transistors. A positive voltage is alternately applied to points (3) and (4) in Figure III-7 so as to alternately turn on transistors Q3 and Q4. When Q3 is conducting, Q4 is nonconducting and vice versa. The voltages applied at points (3) and (4) are derived from a frequency-controlled flip-flop, which is not shown in Figure III-7. As can be seen from the following description, it is by controlling the frequency of this flip-flop that the converter is regulated.

The converter has two independent halves, each of which is capable of operating without the presence of the other. Q1 and Q3 are the active elements of one half; Q2 and Q4 are the active elements of the other half. As previously mentioned, by operating the two halves 180 degrees out of phase, significant reductions are made in the a-c component of the input current and the current in the output filter capacitors. Since the two halves are identical, only the left half is discussed in what follows.

A full cycle of operation of the converter proceeds as follows. Assume that core T3 has just saturated and, therefore, that transistor Q1 has just turned off. Q1 is held off by the voltage appearing across capacitor C1 in parallel with R6 and D9 in its base circuit. The voltage at point (3) is zero at the moment Q1 is turned off. Then, after some predetermined interval of time, depending on the frequency at which the flip-flop as being driven, the flip-flop will be switched and a voltage will be applied at point (3). This turns transistor Q3 on and applies a voltage to winding N1 of core T3 which causes this core to be reset to the opposite saturation level. However, even after core T3 saturates, transistor Q3 continues to conduct. Core T3 is driven well into saturation and maintained in this condition until the flip-flop again reverses states and Q3 is thereby turned off. While Q3 conducts and T3 is saturated, all of the voltage in the reset circuit appears across R2. When the flip-flop switches states and Q3 is turned off, the energy stored in the after-saturation inductance

of transformer T3 causes a voltage to be induced in winding N2 so as to again initiate conduction in Q1.

The conduction interval of Q1 is relatively constant and, in the converter designed under this contract, has been made to be approximately 50 microseconds. The resetting time of core T3 after Q3 is turned on is approximately 40 microseconds. Since the minimum period of the flip-flop circuit has been made to be 100 microseconds, each power transistor can be made to conduct for 50 of every 100 microseconds for a maximum duty cycle of 0.5. Under this condition, either Q1 or Q2 will always be conducting. If the period of the flip-flop is made longer, the duty cycle of the power transistors becomes correspondingly lower. The flip-flop in this particular converter has been designed to be controllable in frequency from a maximum of 10 kc/s to a minimum of 0 c/s in order to provide nondissipative regulation all the way to no load.

Zener diodes D5 and D6 provide voltage clipping at the collectors of the high-speed power transistors Q1 and Q2 such that transient currents caused by the leakage inductance of T1 and T2 do not pass through Q1 and Q2 as they switch abruptly from the conducting to the nonconducting state. By returning the anodes of D5 and D6 to the 28-volt input bus, a small efficiency advantage (about 0.5% in this particular converter) is gained as opposed to using Zener diodes of a higher voltage rating and connecting their anodes to ground. Diosed D7 and D8 prevent D5 and D6 from conducting in the forward direction when Q1 and Q2 turn on.

Resistor R1 and Zener diode D12 are used to provide a convenient voltage level (18 volts) to the reset circuits involving Q3 and Q4.

In order to avoid second breakdown effects in Q3 and Q4, which were observed in preliminary breadboard circuits, it was found to be highly desirable to cause the square-wave voltages at points (A) and (B) to alternate between a positive and a negative value rather than simply between a positive value and zero. By thus providing a fast-risetime reverse voltage to the base-emitter junctions of Q3 and Q4 as they are switched off, second breakdown problems were eliminated. An added precaution, however, is the addition of diodes D10 and D11 and Zener diode D13 to form a voltage clipping network which limits the peak voltage which Q3 or Q4 must withstand to 39 volts.

A single flip-flop is used to control all six stages of this modular converter. Protection is effected by reducing the flip-flop frequency to zero whenever an overload or short circuit occurs. Soft turn on is achieved by a simple circuit which causes the frequency of the flip-flop to rise from zero to its steady-state value at a predetermined rate. These functions and the related subcircuits are described in the following paragraphs.

DESCRIPTION OF OTHER MAIN SUBCIRCUITS

Flip-Flop

A complementary configuration utilizing two NPN and two PNP transistors is used for the flip-flop circuit as shown in Figure III-8. This configuration provides a high degree of temperature stability and protection from false triggering by noise transients. A resistor-diode-capacitor pulse-steering network is used in conjunction with the bases of the NPN pair of transistors to cause the flip-flop to change states each time a pulse is applied to point (11).

The outputs of the flip-flop appearing at points (9) and (10) are applied to the bases of the resetting transistors (Q3 AND Q4) of all six of the building-block converter stages. Capacitors C8 and C9 insure that the bases of these resetting transistors receive a negative voltage rather than merely a near-zero voltage during their nonconducting intervals. Resistors R19 and R21 (and R20 and R22) form a voltage divider which limits the peak-to-peak swing of the flip-flop output voltages to within the emitter-base breakdown voltage limitations of the resetting transistors.

Voltage-to-Pulse-Frequency Converter

The schematic diagram of Figure III-9 shows the regulation and protection circuitry of the Experimental Model. This circuitry can be divided into several main subcircuits. One of these is the voltage-to-pulse-frequency converter involving Q14, UJT1, and Q15. Transistor Q14 and resistor R45 form a voltage-controlled current source and it is the voltage applied to the base of Q14 from the differential amplifier which controls the rate of charging of C19. The charging rate of C19 determines the frequency at which the unijunction transistor UJT1 fires. Transistor Q15 amplifies and inverts the pulses from UJT1 and the output pulses at point (15) are applied to the flip-flop circuit to cause switching.

Differential Amplifier

A matched dual transistor Q13, used as a differential amplifier, compares that percentage of the output voltage provided by the voltage-divider resistors R42 and R43 to the reference voltage derived from Zener diode D23. By connecting R41 and C17 between the two bases of the matched transistor pair Q13, the high frequency gain of the differential amplifier is considerably reduced. This was found to be necessary in order to insure closed-loop stability. Because of C17, the dc gain of the amplifier is undiminished, thus assuring precise steady-state regulation. The value of R41 is chosen to allow the high frequency gain of the amplifier to be great enough to insure that, under transient conditions such as the abrupt removal or application of the load, the overshoot or undershoot of the converter output voltage will be very small.

Protection and Soft-Turn-On Circuits

The converter is designed to "blink off" and return soft on whenever it is overloaded or short circuited rather than simply to current limit.

It will continue to cycle off and on until the overload is removed. Both the length of time the converter remains turned off and the rise time of the output voltage in the Experimental Model are adjustable over a wide range.

The protection circuitry is shown in Figure III-9. The converter output current passes through the current-sensing resistor R33 in such a direction that the bottom of this resistor becomes negative with respect to ground. Whenever the output current exceeds 125% of the rated full load current, Zener diode D18 conducts and transistor Q9 is turned on. This turns on Q11 and the conduction of this transistor reduces the voltage across Zener diodes D21 and D22 to zero, therefore turning off the converter. Transistor Q10 and Q11 form a latching circuit similar to a conventional monostable multivibrator which causes the reference voltage to be held at zero for a predetermined period of time. During the "blink-off interval", transistor Q10 is turned off and transistor Q11 is held on by current through capacitor C13. The blink-off interval ends when C13 becomes fully charged and ceases to allow base current to flow to transistor Q11. The length of this blink-off interval may be adjusted by varying R31 which determines the charging rate of C13.

Soft turn on is accomplished by controlling the rate of charging of capacitor C15 and thereby controlling the rate of rise of the reference-voltage input to the differential amplifier. Adjustment of the soft-turn-on rate is by means of R35 in the base circuit of Q12 through which C15 is charged.

Figure III-10 shows the interconnection of the various subcircuits discussed herein. The numbers on the connection points refer to numbers on these same points in the subcircuit schematics of Figures III-7, III-8, and III-9. A parts list for the Experimental Model is given in Appendix A.

REFERENCES

4. See end of Section I.

6. INVERTER FOR USE WITH VERY LOW INPUT VOLTAGES, E. T. Moore and T. G. Wilson, IEEE Transactions on Communications and Electronics, VOL. 83, July, 1964, pp. 424-428.

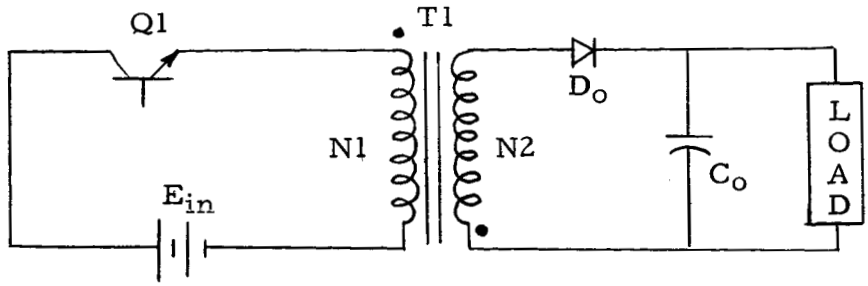


FIGURE III-1. CIRCUIT ILLUSTRATING BASIC PRINCIPLES OF D-C TO D-C CONVERSION THROUGH AN ENERGY-STORAGE TRANSFORMER.

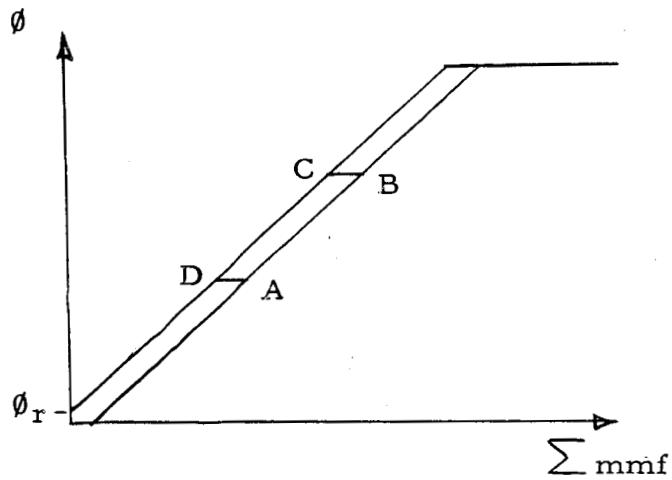
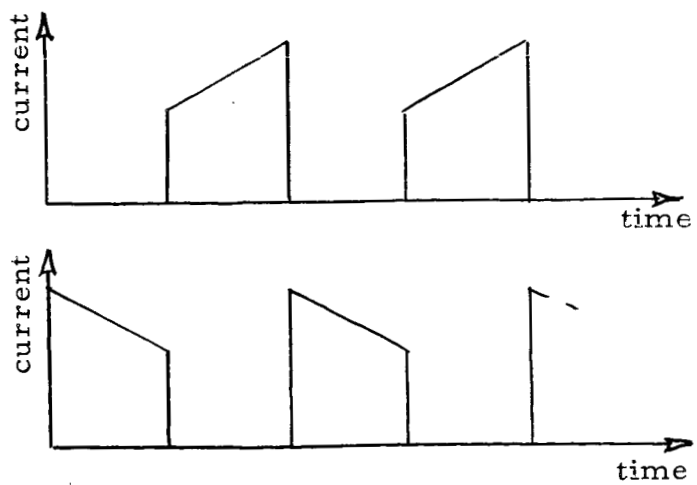


FIGURE III-2. MAGNETIC CHARACTERISTICS OF CORE T1 OF FIGURE III-1.



(A)

(B)

FIGURE III-3. (A) CURRENT VS. TIME THROUGH Q1 IN FIGURE III-1.
(B) CURRENT VS. TIME THROUGH D_o IN FIGURE III-1.

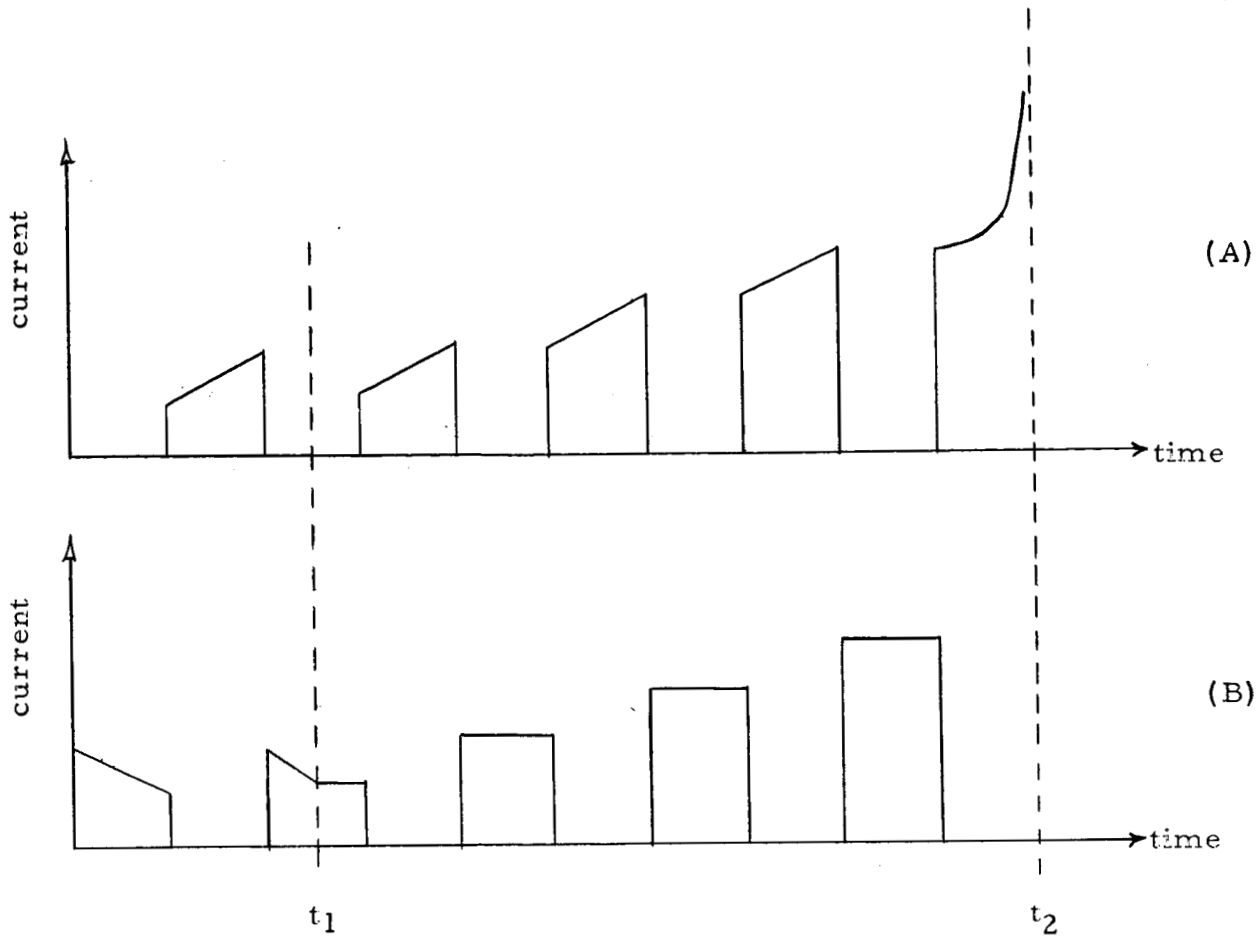


FIGURE III-4. (A) BUILD UP IN CURRENT VS. TIME FOR TRANSISTOR Q_1 IN FIGURE III-1 AFTER LOAD SHORT CIRCUIT WHICH OCCURS AT TIME t_1, ASSUMING NO PROTECTION ACTIONS ARE TAKEN.
(B) BUILD UP IN CURRENT VS. TIME FOR DIODE D_o IN FIGURE III-1 AFTER LOAD SHORT CIRCUIT WHICH OCCURS AT TIME t_1, ASSUMING NO PROTECTION ACTIONS ARE TAKEN.

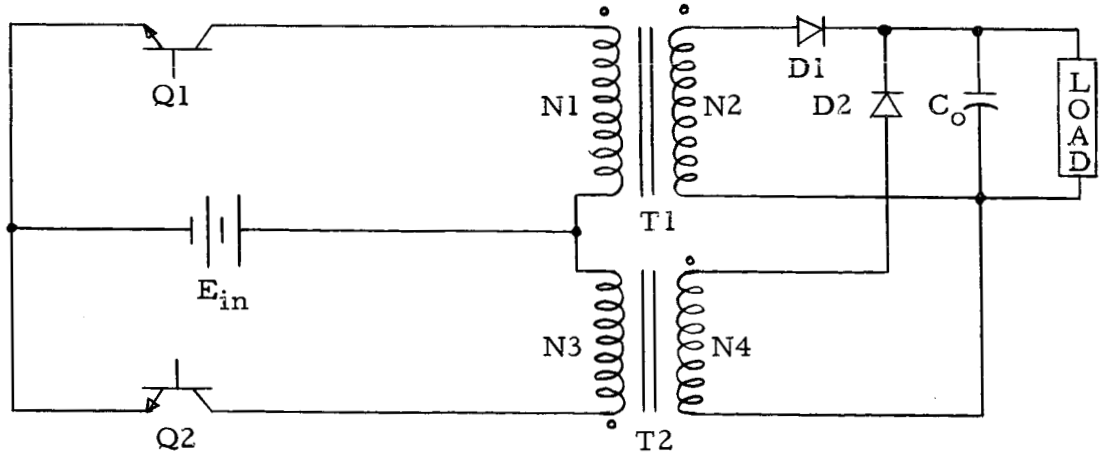


FIGURE III-5. BASIC FULL-WAVE CONFIGURATION OF THE "ENERGY-PUMPING" CONVERTER.

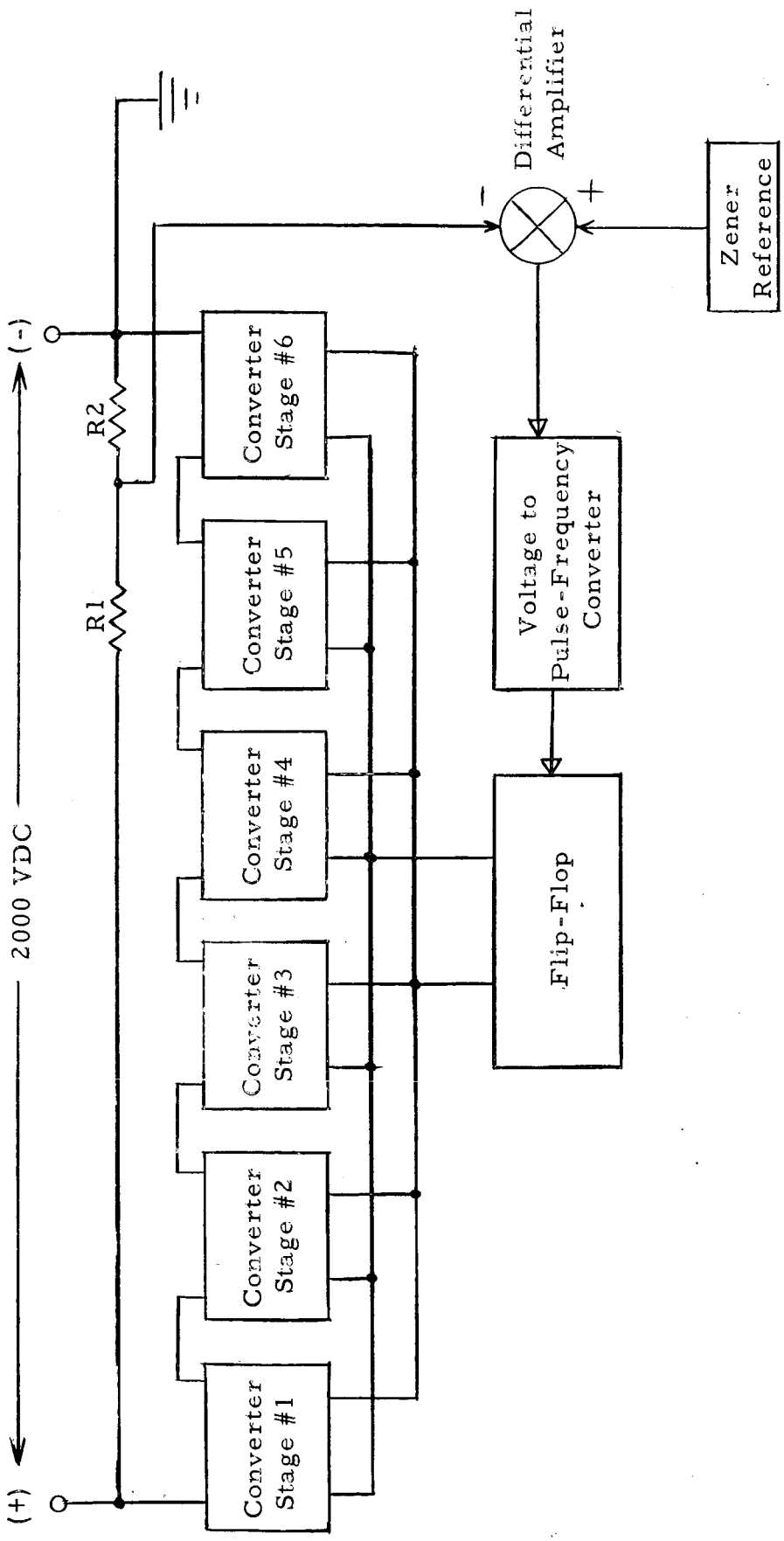


FIGURE III-6. BLOCK DIAGRAM OF THE COMPLETE CONVERTER. The six identical building-block stages are connected with their inputs in parallel (not shown) and their outputs in series as shown above.

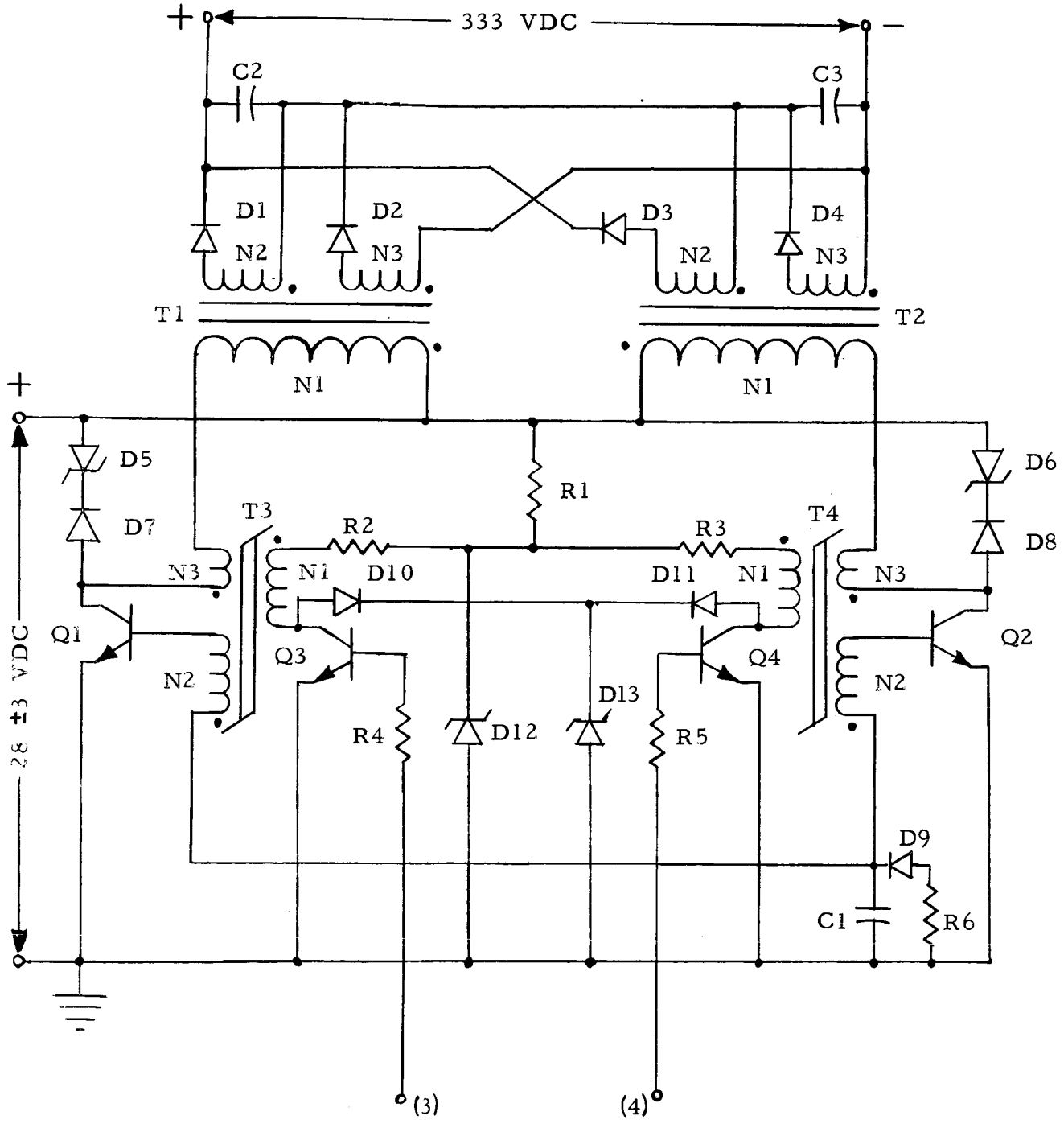


FIGURE III-7. THE BUILDING-BLOCK CONVERTER STAGE. Six of these stages are used in the modular 1600-watt dc to dc converter.

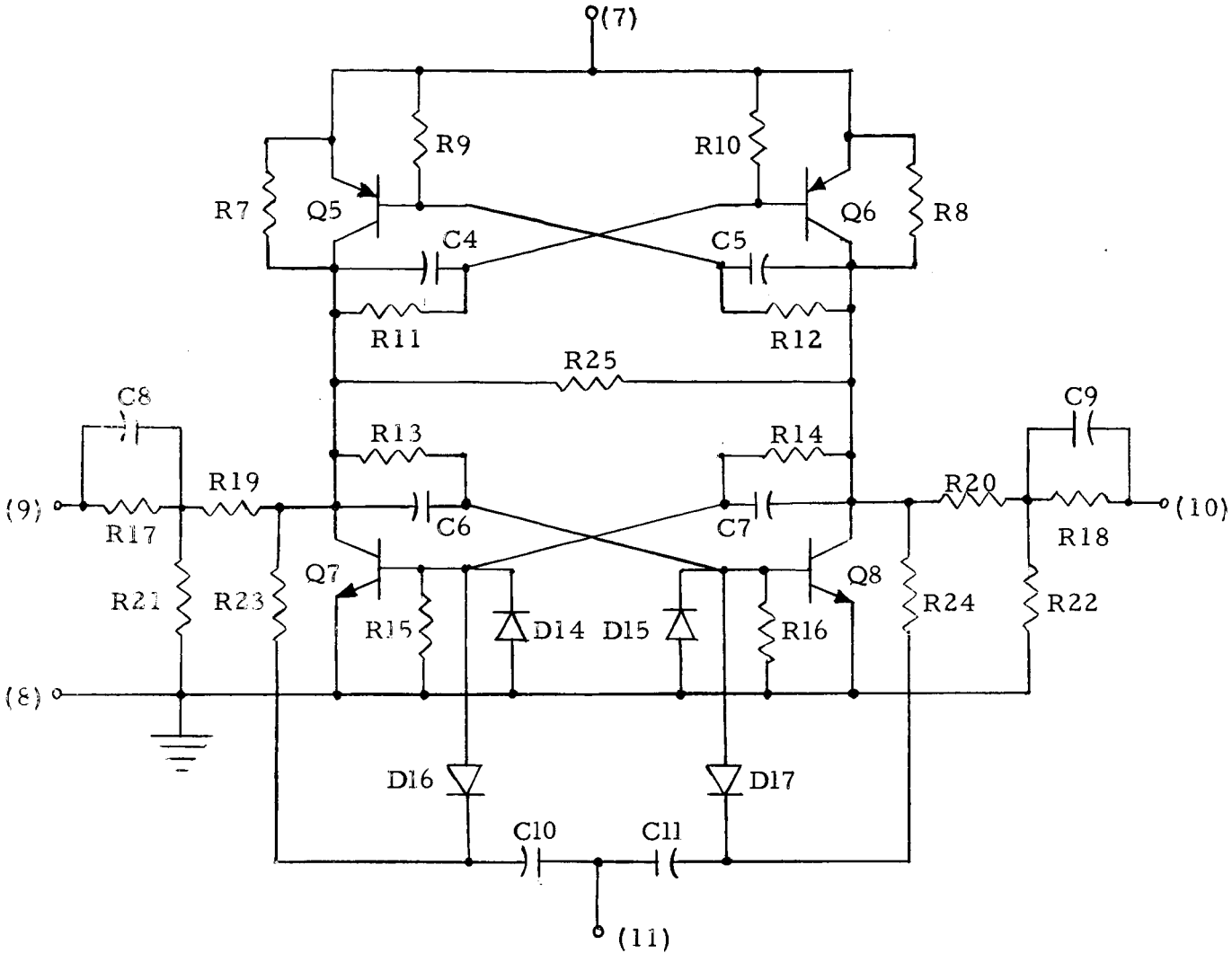


FIGURE III-8. THE FLIP-FLOP CIRCUIT. The frequency with which this flip-flop reverses states is determined by the frequency of the pulses applied to the flip-flop at point (11). The output voltages of the flip-flop points (9) and (10) are applied to all six building-block converter stages.

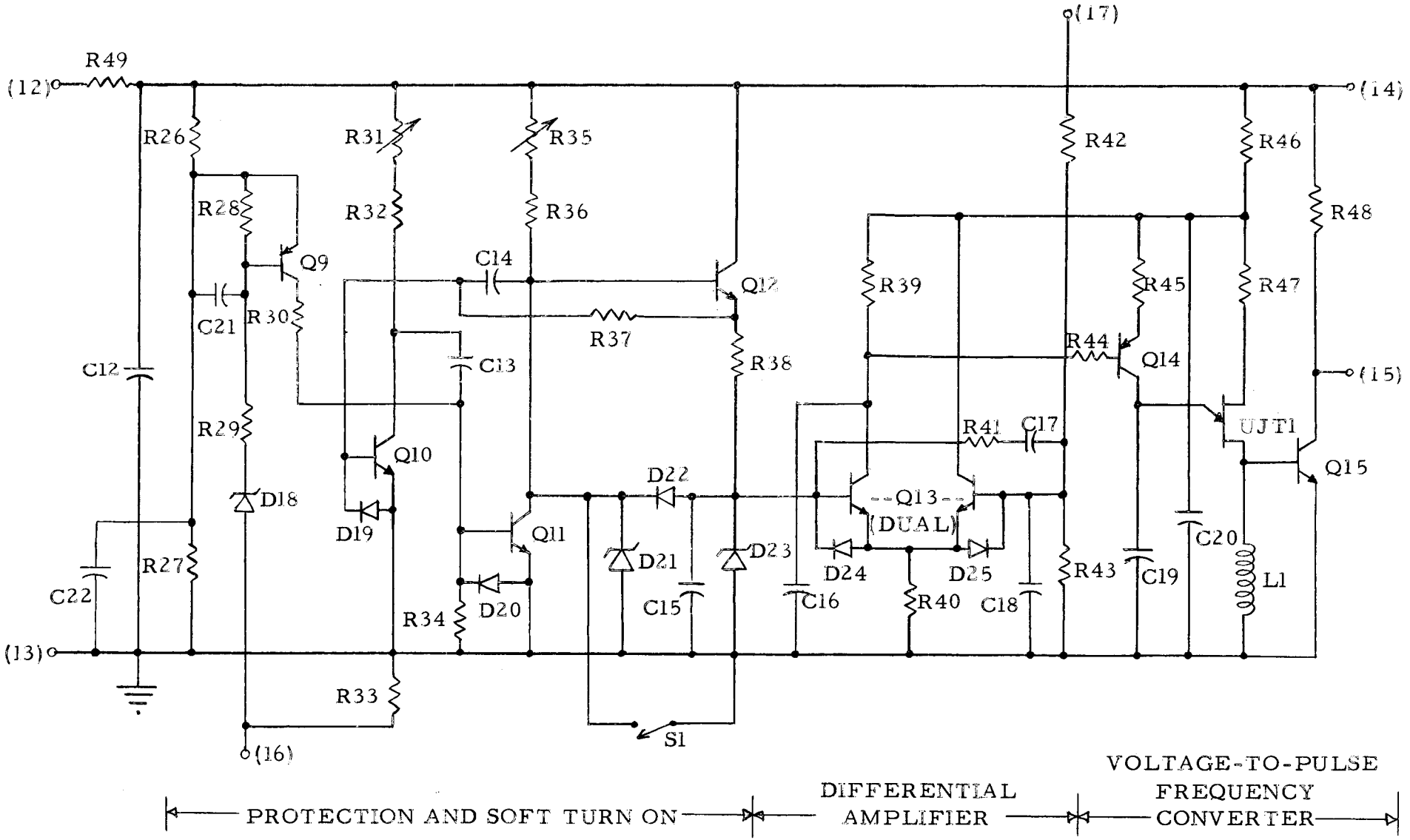


FIGURE III-9. REGULATION AND PROTECTION CIRCUITRY

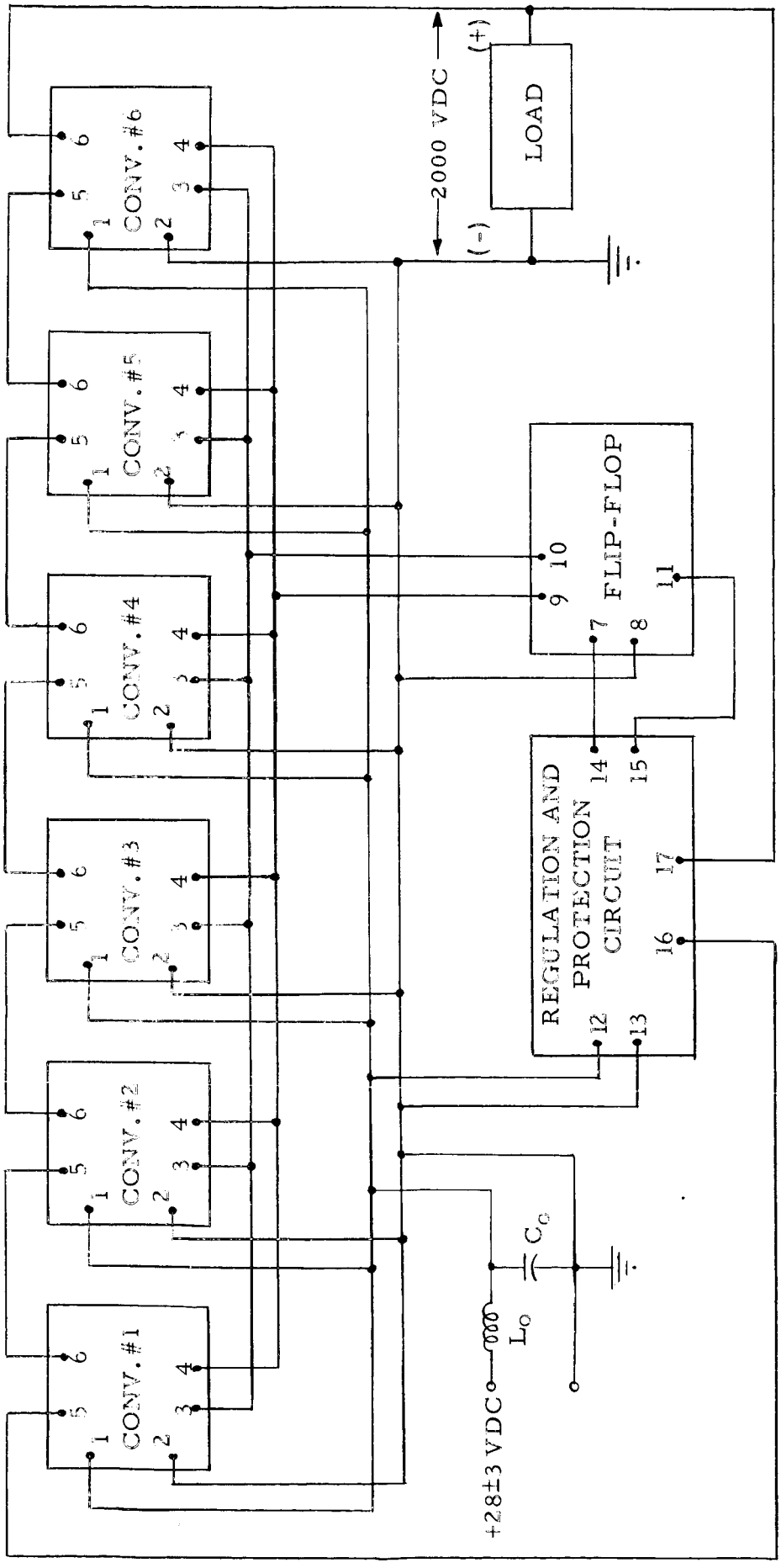


FIGURE III-10. WIRING DIAGRAM SHOWING INTERCONNECTION OF SUBCIRCUITS OF THE EXPERIMENTAL MODEL. Numbers on connection points refer to numbers on these same points in the subcircuit schematics of Figures III-7, III-8, and III-9.

IV. PERFORMANCE AND WEIGHT OF THE EXPERIMENTAL MODEL

During the testing program, the Experimental Model was operated for more than 15 hours, including 10 hours of continuous operation. Using a hydrogen thyratron as a breakdown device in parallel with the load, the converter was subjected to more than 100,000 severe thyratron-induced load transients. The load was also directly short circuited approximately 200 times with a metallic conductor. No failures or performance degradation resulted from any of these tests. The general performance of the converter is outlined below in considerable detail.

EFFICIENCY

The maximum efficiency of the converter was found to be 88.8%, and this occurs at 64% of full load. With a 28-volt input, the full load efficiency is 86.5%.

Figure IV-1 shows the curve of efficiency vs. load current with the input voltage held constant at 28 volts.

Figure IV-2 shows curves of efficiency vs. input voltage over the range of 25 to 31 volts. Curves are shown for 34%, 64%, and 100% of full load.

REGULATION

Regulation from no load and an input voltage of 31 volts to full load and an input voltage of 25 volts was found to be $\pm 0.45\%$. Most of this slight output voltage variation was observed to occur from no load to 25% of rated load. This degree of regulation is an order of magnitude better than the $\pm 5\%$ specified in the contract. However, the extra precision of regulation is achieved in a manner which does not decrease the converter efficiency or increase the converter weight or complexity.

RIPPLE

The maximum RMS voltage ripple in the 2000-volt output of the converter was found to be less than 4 volts or less than 0.2%. An oscilloscope picture of the waveform of this ripple under full-load conditions is shown in Figure IV-3.

Figure IV-4 shows an oscilloscope picture of the waveform of the current drawn from the source by the converter. As specified in the contract, the RMS value of the ripple current from the source at full load is limited by the choke-capacitor input filter of the converter to less than 2% of the average value of the input current. The actual RMS value of this ripple current is approximately 1%. The high-frequency spikes which are evident in the waveform of Figure IV-4 were extraneous pickup by the probe and its leads. (This could be demonstrated in the test configuration by physically moving the probe, shortening and rearranging its leads, etc.)

Disregarding these high-frequency spikes, the peak current drawn from the source at full load is less than 2% greater than the average value of the source current.

ADJUSTABLE SOFT-TURN-ON AND BLINK-OFF TIMES

By adjusting potentiometer R35 (see Figure III-9), the rise time of the output voltage of the Experimental Model can be set anywhere in the range from 20 milliseconds to 520 milliseconds. Further adjustment in the direction of decreasing rise time requires that the value of resistor R36 be changed. The energy-storage-transformer converter, however, has an inherent soft turn on characteristic which establishes a minimum rise time of approximately 8 milliseconds. No such limit exists insofar as lengthening the soft turn on rise time is concerned. The maximum rise time can be increased by adding capacitance in parallel with C15 (see Figure III-9).

Figure IV-5 shows oscilloscope traces taken from the Experimental Model of the rise of output voltage with the soft-turn-on potentiometer adjusted for minimum and maximum rise time.

The "blink-off time", or time interval that the converter remains turned off before attempting to turn on again after an overload has activated the protection system, is adjustable by means of potentiometer R31 (see Figure III-9). In the Experimental Model, adjustment of R31 varies the blink-off time between 20 and 100 milliseconds. These limits on the blink-off time may be decreased or increased by changing the value of C13.

VOLTAGE AND CURRENT WAVEFORMS AND POWER DISSIPATION FOR MAIN COMPONENTS

Figure IV-8 shows the cyclic waveform of the collector-emitter voltage of one of the MHT8302 power transistors (Q1, Q2) of the Experimental Model at full load. During their nonconducting interval, these transistors are required to block a voltage of twice the input voltage or approximately 56 volts. As one of these high-speed power transistors turns off a voltage transient from collector to emitter, lasting approximately 0.8 microsecond, occurs because of the small leakage inductance of the energy-storage transformers (T1, T2). This voltage spike is evident in Figure IV-8 and is seen to have an amplitude of 80 volts. As mentioned in Section III, the amplitude of this voltage transient is limited to this value by Zener diodes D5 and D6.

That the increment of inductive energy stored in the leakage inductance of each energy storage transformer is diverted from the main power transistors as they abruptly assume their high impedance state is illustrated in Figure IV-9. This oscilloscope trace shows the current pulse through one of the voltage-clipping Zener diodes (D5, D6) when the power transistor associated with this diode turns off. This current flowing through an 80-volt potential for approximately one microsecond each cycle is roughly equivalent

to one percent of the output power. As mentioned previously, by connecting the anodes of the clipping Zener diodes to the positive terminal of the converter input filter capacitors rather than using higher voltage Zener diodes and connecting their anodes to ground, part of this inductive energy is recovered and a significant efficiency advantage is obtained.

Figures IV-10 and IV-11 show the very short rise and fall times of the current switched by the high-speed MHT8302 power transistors. Even at 10 kc, switching losses are a minor portion of the dissipation in these transistors and, except for other considerations such as the losses in the magnetic components, a considerably higher operating frequency, e.g. 20 kc, could have been used.

Figure IV-12 shows the steady-state waveform of the collector current of a converter power transistor at full load. Figure IV-13 shows the corresponding waveform of the current through one of the output rectifiers. These waveforms compare remarkably well to the idealized waveforms for these currents as shown in Figure III-3.

One problem existing in the Experimental Model is illustrated in Figures IV-6 and IV-7. This problem involves a high voltage transient which occurs across the output rectifiers D1-D4 (see Figure III-7) as they cease to conduct current in the forward direction and begin to block a reverse voltage. This high voltage transient is shown in the oscilloscope picture of Figure IV-6 and is seen to reach a peak value of 1,000 volts. The forward and reverse current through this rectifier during its recovery interval is shown in Figure IV-7. The reason for the high voltage transient across the rectifier is that, as the voltage across the rectifier reverses, the rectifier at first conducts a relatively large current in the reverse direction and then very abruptly begins to block this current. When this reverse current is "snapped off", the slight leakage inductance of the secondary winding of the energy-storage transformer causes a large voltage transient to appear across the rectifier. The peak magnitude of this voltage transient can be limited by either of two phenomena: (1) reverse breakdown of the diode or (2) the winding capacitance of the secondary of the energy-storage transformer.

The 1000-volt transient to which for fractions of a microsecond the output rectifiers are subjected is a serious problem. The rectifiers used in the Experimental Model are parallel pairs of 2-ampere, 600-volt devices by Unitrode and are not avalanche breakdown types. It is recommended that Unitrode's new 4-ampere, avalanche-breakdown, fast recovery rectifiers be used in any subsequent models of this converter, and that consideration be given to the use of pairs of these avalanche-breakdown devices in series.

Appendix C gives the voltages, currents, and power dissipations to which the main power-handling converter components are subjected.

PROTECTION

One of the advantages of the energy-storage-transformer converter is that extraction of energy from the source occurs on one half cycle and delivery of this energy to the output filter capacitors and load occurs on the next half cycle. Excellent protection characteristics are made possible by the fact that there is never a direct energy-transfer path between the source and the load. Short circuiting the load causes no current transients through either the power transistors of the converter or the output rectifiers. This fact is illustrated for the output rectifiers by the oscilloscope trace shown in Figure IV-14.

As mentioned previously, while operating at full load the Experimental Model was subjected to more than 100,000 severe thyratron-induced load transients and to more than 200 direct short circuits of the load with a metal conductor. No damage or degradation occurred.

In connection with the protection characteristics of this converter it is interesting also to note the results of short circuit tests which were performed on the breadboard model with its protection system completely disabled. Short circuits sustained for periods of up to 4 seconds were found to cause no component failures. This was the longest period for which the unprotected converter was short circuited. This unusual ruggedness is attributable to the characteristics of the energy-storage transformers and to the current-feedback system of base drive. The Experimental Model was not subjected to short circuits with its protection system disabled; however, it would be expected to display the same degree of ruggedness.

WEIGHT

the total weight of the components of the Experimental Model is 16.43 pounds. The weight of the energy-storage transformers comprises 58.4 percent of this total. The weights of other components and their relative percentage of the total are listed in Table IV-1. Certain possible improvements to the converter, several of which would result in a reduced weight, are discussed in Section V.

TABLE IV - 1. COMPONENT WEIGHT ANALYSIS

Component Description	Qty.	Weight per Item (lbs.)	Total wt. of Comp. Type (lbs.)	% of All Component Weight
Power Transformer	12	0.80	9.60	58.4
Output Filter Capacitor	12	0.20	2.40	14.6
Input Filter Capacitor	3	0.61	1.83	11.1
Power Transistor	12	0.07	0.84	5.1
Input Choke	1	0.68	0.68	4.1
Current Transformer	12	0.03	0.36	2.2
All Other Components			0.72	4.4
TOTAL			16.43	100.0

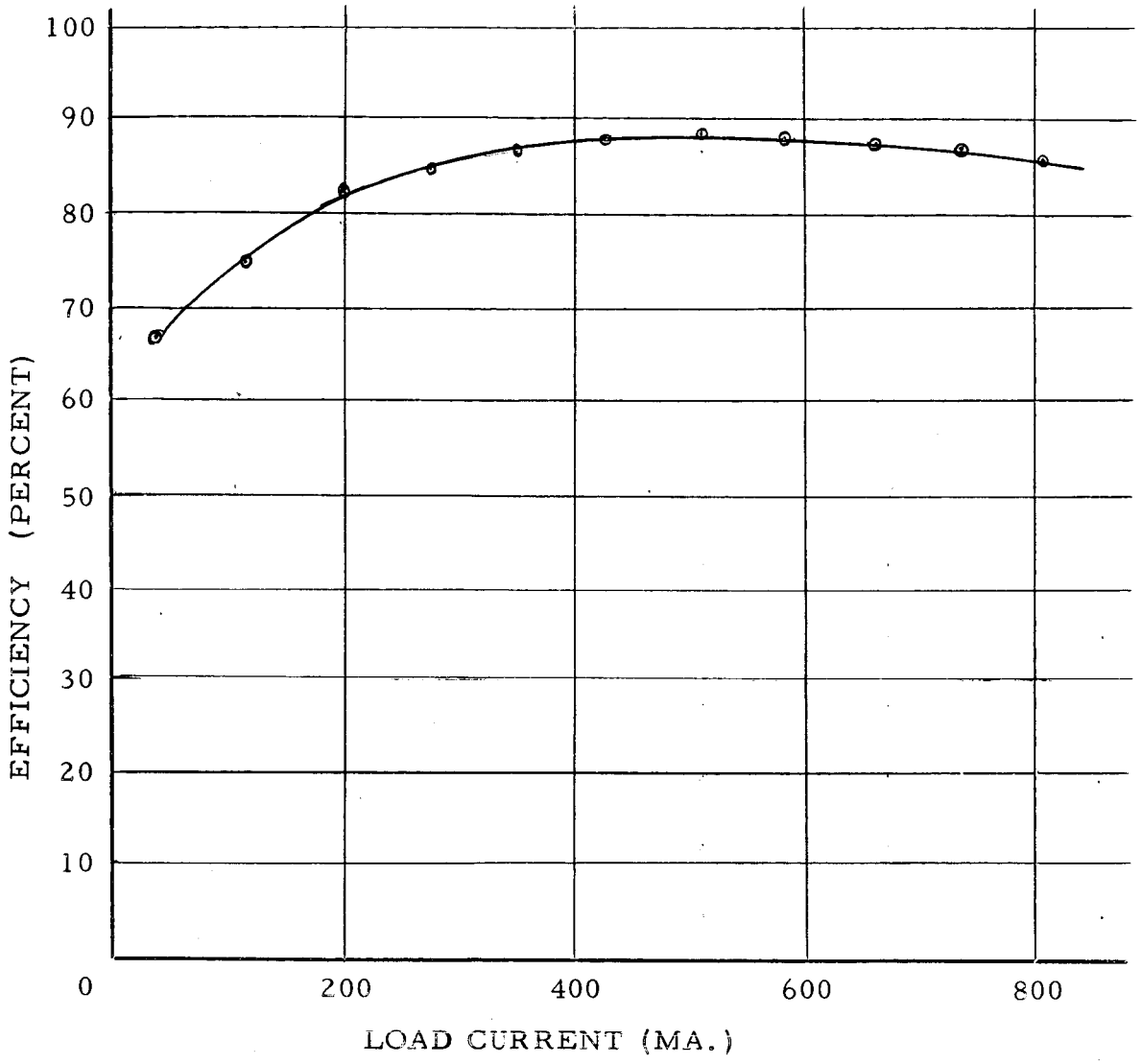


Figure IV - 1. EFFICIENCY VS. LOAD CURRENT FOR AN INPUT VOLTAGE OF 28 VOLTS

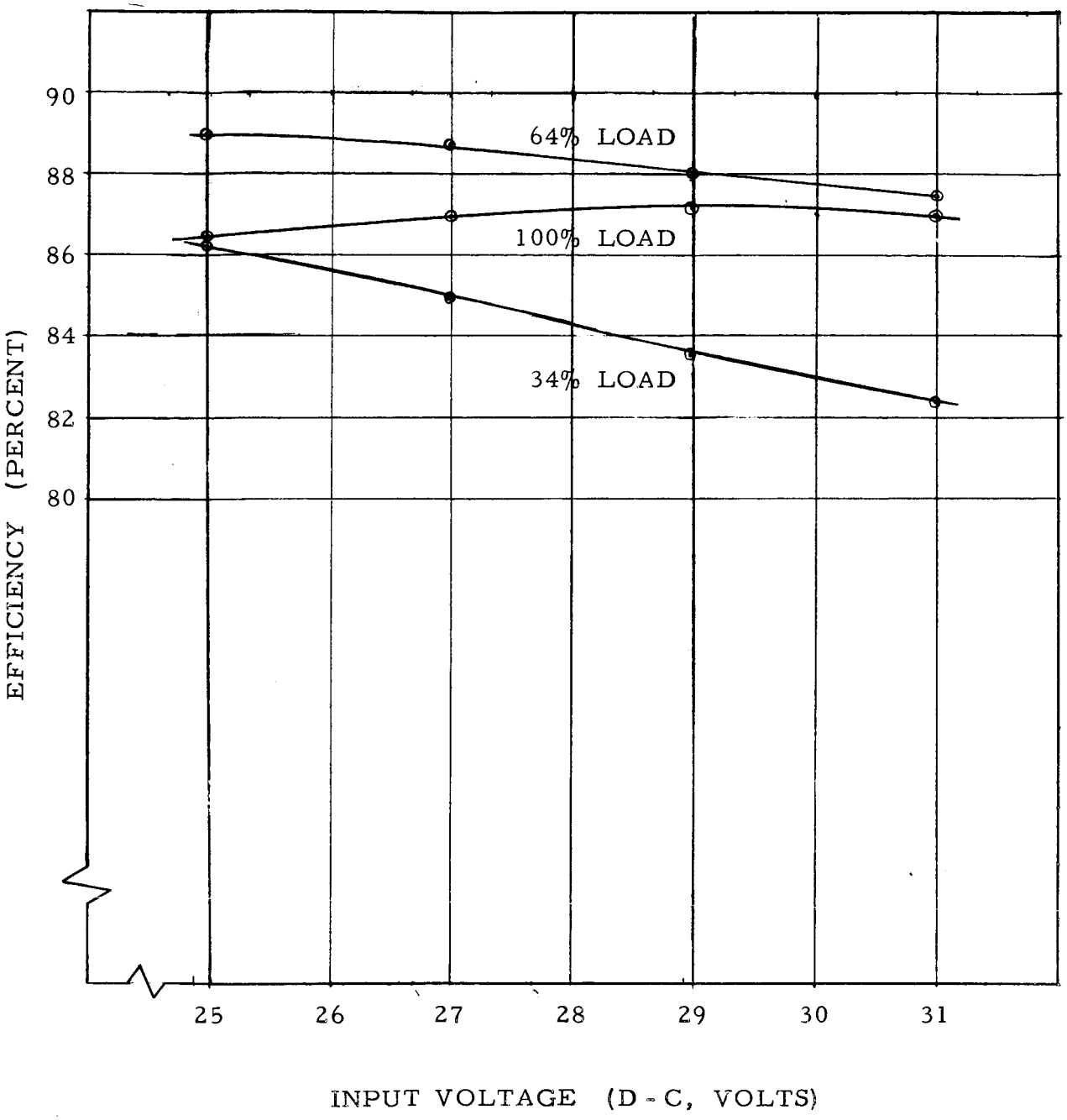


FIGURE IV - 2. EFFICIENCY VS. INPUT VOLTAGE. Curves are shown for conditions in which load current is held constant at 34%, 64% and 100% of the full load value of 800 milliamperes.

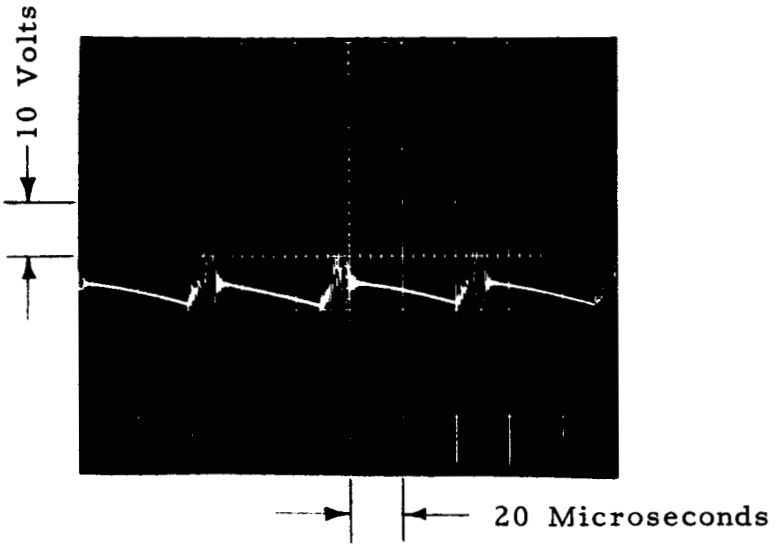


FIGURE IV - 3. OUTPUT VOLTAGE RIPPLE AT FULL LOAD

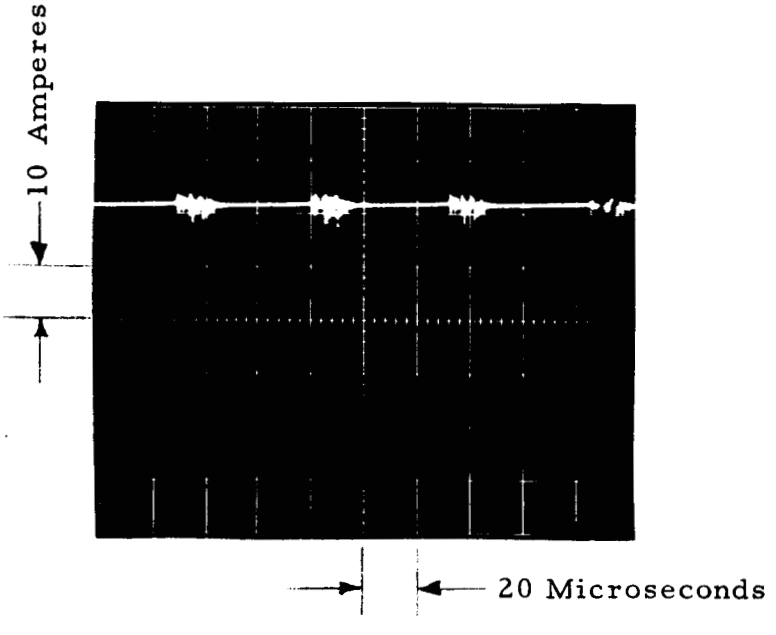


FIGURE IV - 4. INPUT CURRENT RIPPLE AT FULL LOAD

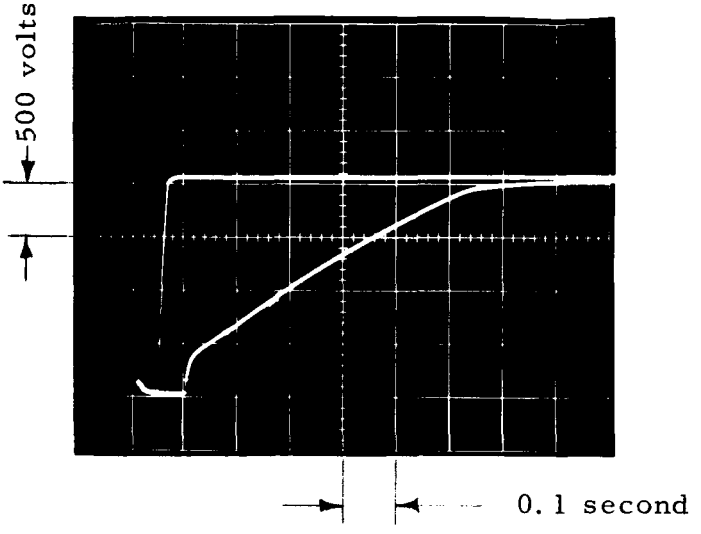


FIGURE IV - 5. RISE OF OUTPUT VOLTAGE SHOWING SOFT TURN ON CHARACTERISTICS. The upper trace shows the rise of output voltage when the potentiometer which adjusts the soft turn on is set for minimum rise time. The lower trace shows the same waveform for the setting which provides maximum rise time.

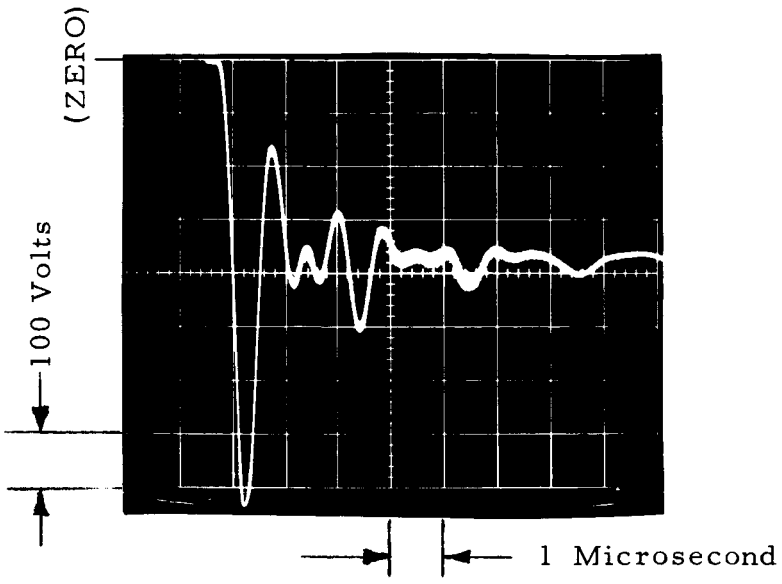


FIGURE IV - 6. VOLTAGE ACROSS AN OUTPUT RECTIFIER (UNITRODE UTR - 62) DURING RECOVERY INTERVAL.

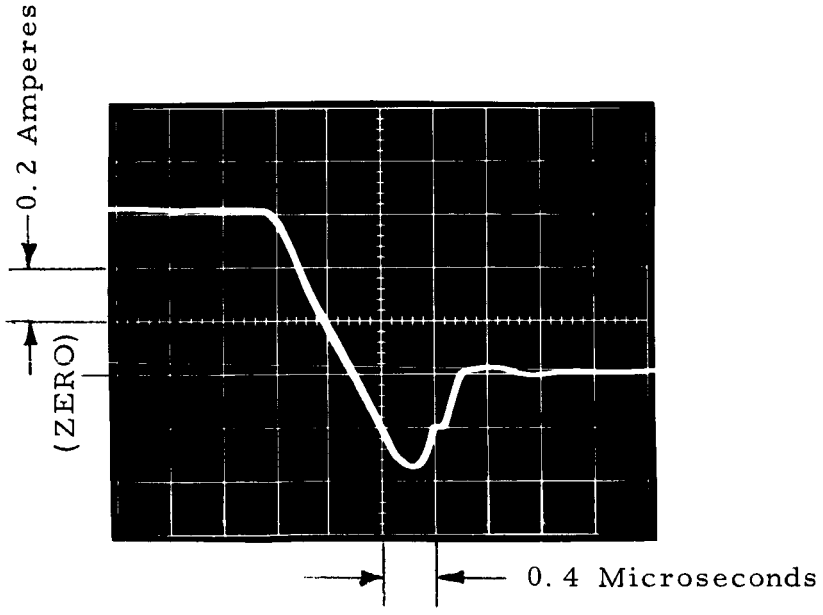


FIGURE IV - 7. CURRENT THROUGH AN OUTPUT RECTIFIER (UNITRODE UTR - 62) DURING RECOVERY INTERVAL.

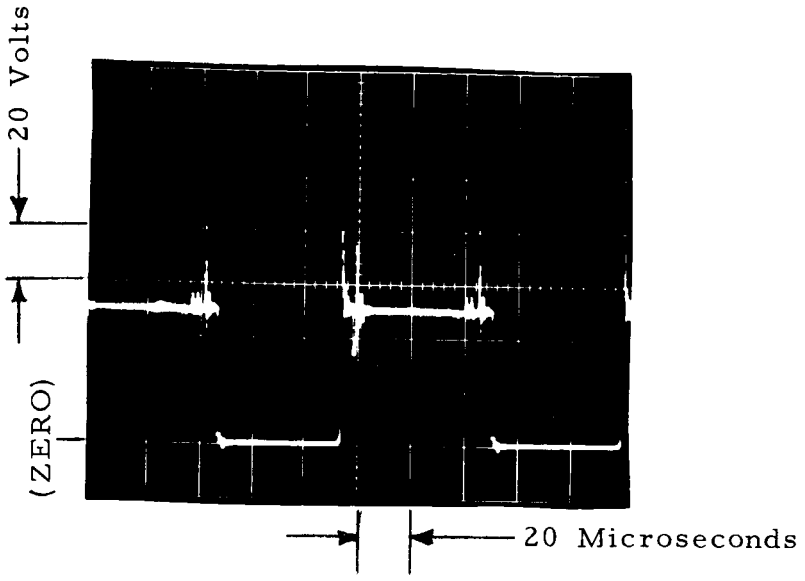


FIGURE IV - 8. COLLECTOR - EMITTER VOLTAGE OF MHT 8302 POWER TRANSISTOR.

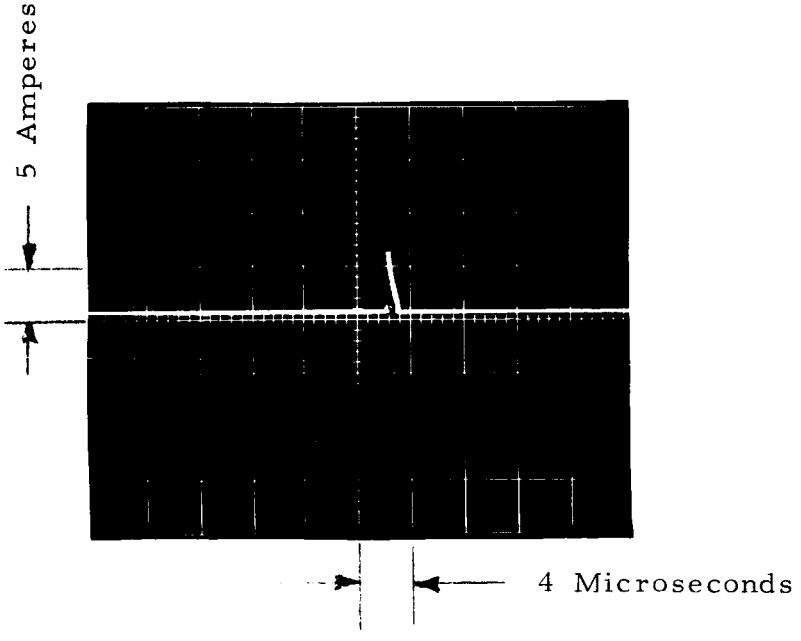


FIGURE IV - 9. PULSE OF CURRENT THROUGH THE 1N2991B ZENER DIODE WHEN THE POWER TRANSISTOR TURNS OFF UNDER FULL - LOAD CONDITIONS.

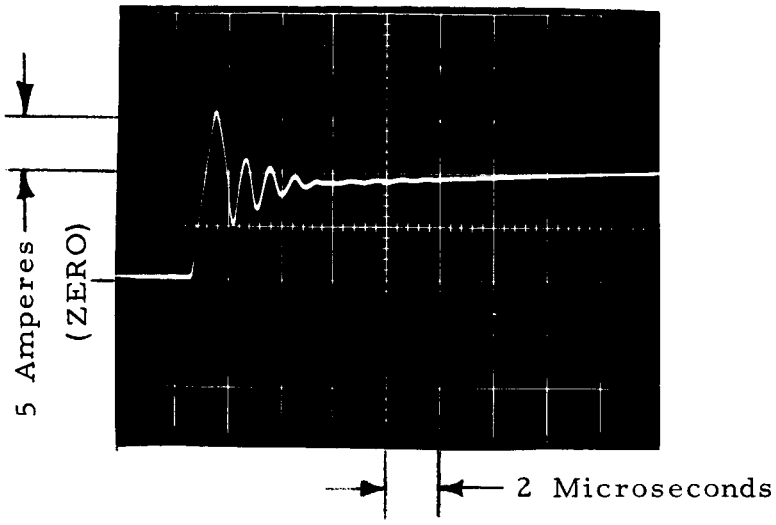


FIGURE IV - 10. COLLECTOR CURRENT OF MHT 8302 POWER TRANSISTOR DURING TURN-ON INTERVAL. This waveform does not reflect the rise-time characteristics of the power transistor so much as it does the effective series inductance of the transformer winding connected in series with the transistor.

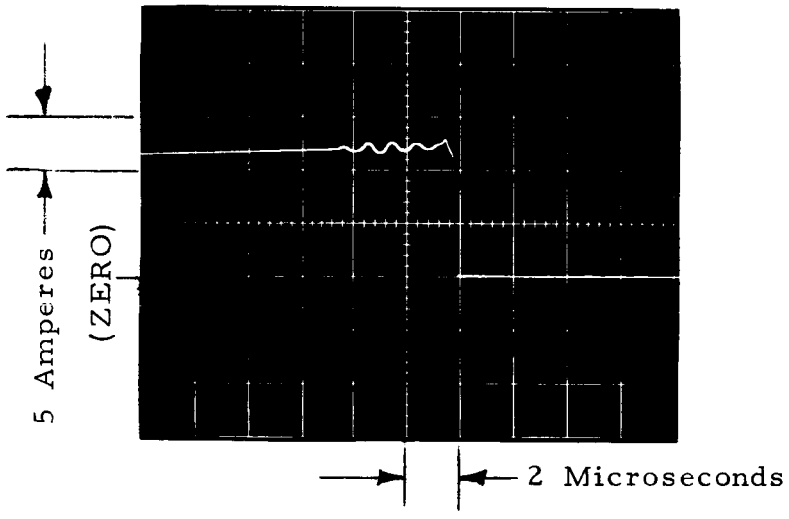


FIGURE IV - 11. COLLECTOR CURRENT OF MHT 8302 POWER TRANSISTOR DURING TURN-OFF INTERVAL. This waveform shows relatively accurately the very short fall time of the current through the power transistor since reactive current resulting from external circuit inductance is bypassed by the 1N2991 Zener diode (See Figure IV - 9).

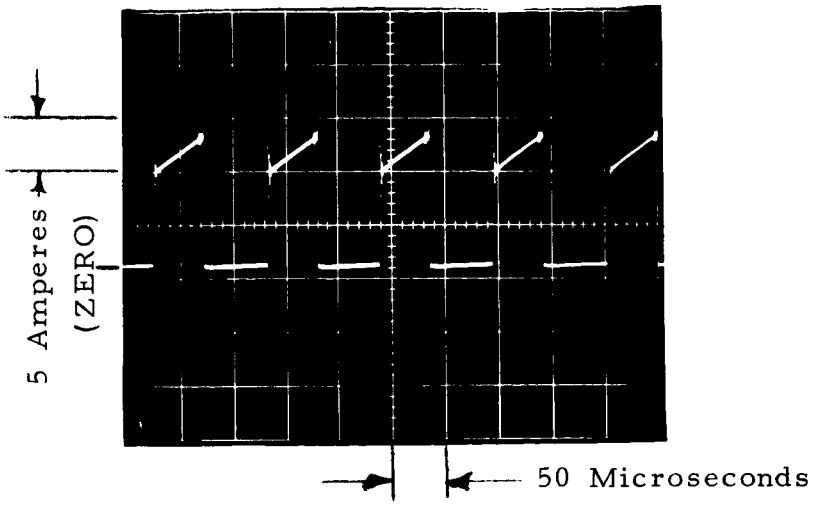


FIGURE IV - 12. STEADY-STATE WAVEFORM OF THE COLLECTOR CURRENT OF A MHT8302 POWER TRANSISTOR AT FULL LOAD.*

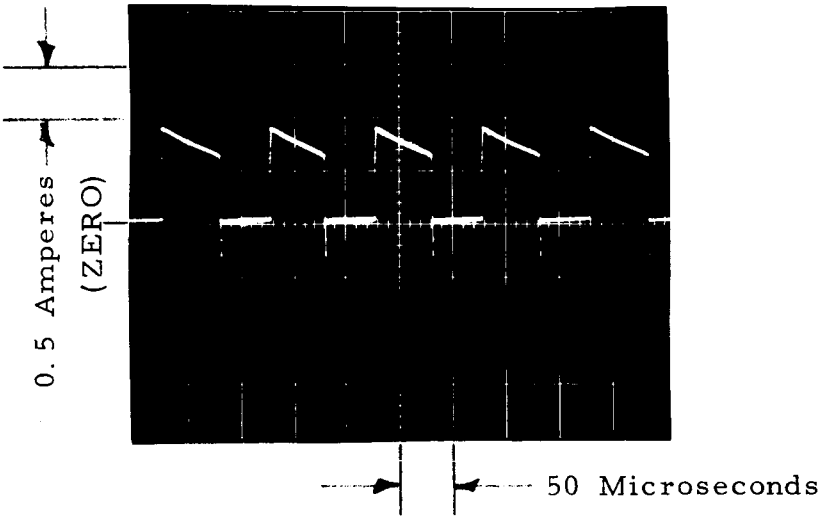


FIGURE IV - 13. STEADY-STATE WAVEFORM OF THE CURRENT THROUGH A UTR-62 OUTPUT RECTIFIER AT FULL LOAD.*

* The slight tilt in the zero levels of these current waveforms is caused by the limited low frequency response of the Tektronix type P6016 current probe with passive termination which, with appropriate d-c bias, was used to record these waveforms.

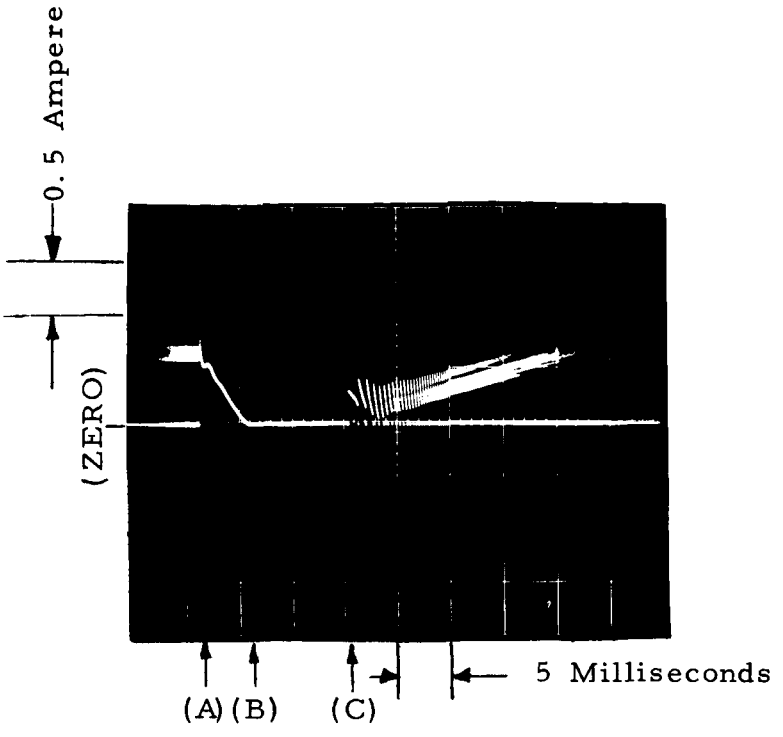


FIGURE IV - 14. CURRENT THROUGH A UTR-62 OUTPUT RECTIFIER AS THE CONVERTER IS SUBJECTED TO A SEVERE OVERLOAD BY THE FIRING OF A THYRATRON CONNECTED IN PARALLEL WITH THE LOAD. Prior to point (A) on the time scale of the above picture, the converter was operating under steady-state conditions. At point (A) the hydrogen thyratron was fired. Note the absence of any current surge through the rectifier. Because of the overload, the converter protection system is actuated and at point (B) the rectifier current has reached zero and the thyratron begins to recover its blocking ability. At point (C) the converter "blink-off" period ends and "soft turn on" of the converter begins.

V. POSSIBLE IMPROVEMENTS

The research and development effort under this contract has established a basic design and verified certain desirable features of the energy-storage transformer approach. An Experimental Model of a lightweight, highly efficient modular converter using this approach has been built and tested. As a result of this work, much has been learned about the design and performance of this type of dc to dc converter. Also, since this work was initiated, new high voltage power transistors have been made available which would seem to have certain advantages in this converter. It is felt that the present converter design can be improved and refined such that a somewhat lighter, more efficient converter than the present Experimental Model can be built. Certain specific improvements are suggested below.

PER-STAGE PROTECTION

The converter designed under this contract uses a modular approach. Six identical building-block stages are used with the output voltage of each stage being nondissipatively controllable. This approach contrasts with other modular schemes which involve, for example, several unregulated stages plus one stage which has a controllable output voltage and which is used to regulate the composite system. The use of identical building-block stages rather than regulated and unregulated stages has the advantage of allowing the design of a protection system such that the failure of any one stage would not prevent the converter from continuing to supply not only full power but also the normal regulated voltage to the load. The use of identical building-block stages has the further advantage of greatly facilitating the scaling up or down of power or voltage levels in modular converters using these stages as building blocks. The potential disadvantage of such a system, i.e. a modular system in which all building-slock stages are regulated and exactly identical, is that providing the means for nondissipatively controlling the output voltage of each stage may introduce additional complexity. However, the techniques developed under this contract allow this to be accomplished with little or no added complexity.

The six-stage modular converter developed under this contract was designed such that any five of the six building-block stages could provide the full output power and maintian normal voltage regulation. Loss of any one stage would merely involve a 20% increase in the voltage and power delivered by the other five stages. The main effect on system performance would be a slight drop in efficiency.

However, in order to take advantage of the reliability advantage made possible by this capability, the present overall protection system of the six-stage converter must be supplemented by a "per-stage protection system" for each individual stage. The per-stage protection system of an indivual stage would perform the function of turning off that stage in the event of a malfunction within that stage which, for example, caused that stage to draw an

input current of more than 150% of the maximum current it would normally require at full load.

Although the design of such per-stage protection systems was not a part of this contract, some work was done in this direction. A system was developed which worked well with breadboard models of individual stages but which was found to be unsatisfactory when tested in the full six-stage converter. The Experimental Model actually contains the components for these per-stage protection systems but these systems have been disabled as they were found to perform unsatisfactorily. (The components of these disabled per-stage protection systems in the Experimental Model are painted blue for easy identification and to give a visual indication of the amount of complexity they add.)

The development and testing of a simple and reliable per-stage protection system could readily be accomplished and, in fact, has already been started as mentioned above. It is recommended that this be carried out as it significantly enhances the advantages of the modular design approach.

USE OF AVALANCHE RECTIFIERS

As discussed in Section IV the abrupt recovery characteristics of the output rectifiers in the building-block converter stages creates an inductive voltage spike which was found during the testing program to have a sufficient magnitude to pose a definite hazard to the parallel pairs of Unitrode UTR-62 diodes now being used as output rectifiers. A first step toward eliminating this problem would be to substitute for the UTR-62 diodes a diode which would have avalanche breakdown characteristics and a higher dissipation rating. The new UTR-63 fast-recovery, avalanche-breakdown, 3-ampere diode recently made available by the Unitrode Corporation should be evaluated for this purpose. It may be found to be desirable to use pairs of these diodes in series.

WEIGHT REDUCTION

Energy-Storage Transformers

The present Experimental Model was designed such that the cyclic change of flux in the energy-storage transformer is equal to approximately 15% of the saturation-flux level of the cores. Based on the performance of this converter and the design information resulting from the work to date, it appears to be possible to use somewhat smaller energy-storage transformers for the same power level by utilizing a higher-percentage cyclic change of flux. Specifically, it is suggested that a cyclic flux change equal to approximately 25% of the saturation-flux level be used for the energy-storage transformers of future versions of this converter. This would result in a theoretical weight savings of 40% for the energy-storage transformers and an estimated actual savings of 30%. Since these transformers comprise

58.4% of the total weight of the converter components, the overall component weight of the converter would thereby be reduced by approximately 18.5%. Slightly higher eddy current losses would occur in the smaller cores because of the greater rate of flux change per unit of core area. However, the volume of the cores would be reduced and copper losses also would be reduced. It is estimated that the net decrease in converter efficiency would be approximately 0.4%.

Output Filter Capacitors

The twelve 22 microfarad output filter capacitors together represent 14.6% of the total component weight of the converter. Insofar as meeting the output-voltage ripple requirement of 5% (RMS) is concerned, these capacitors are excessively large. As mentioned in Section IV, the full load output ripple with these capacitors is less than 0.2%. The value of the output filter capacitors was selected not only on the basis of adequate ripple attenuation but also from condiseration of the maximum ac current which flows through these capacitors and the resulting internal heating. However, it is suggested on the basis of tests and evaluation to date that the value of the output filter capacitors should be reduced from 22 microfarads to the range of 10 - 14 microfarads. The total component weight of the converter should be reduced approximately 5% by this change and the output ripple voltage (RMS) should still be less than 1%.

Input Filter

It should be noted that computer-grade aluminum electrolytic capacitors rather than tantalum capacitors were used in the LC input filter of the Experimental Model because of the very high cost of suitable tantalum types, although the tantalum capacitors would have better temperature characteristics and would weigh less.

In order to limit the ripple in the source current to 2% (RMS) when the source has an extremely low internal impedance such as the storage batteries and laboratory power supplies with which the Experimental Model was tested, an inductor-capacitor input filter is necessary. If, for example, the source has a zero internal impedance, the use of a simple capacitor input filter will have no effect at all upon the source ripple current. However, a solar-cell array is characterized by a significant internal impedance. It is suggested that the input-filter requirements be analysed on the basis of the characteristics of a solar-cell cource and that it may be desirable to eliminate the input inductor or to make it much smaller.

USE OF A HIGHER INPUT VOLTAGE

The choice of 28 volts as the nominal input voltage for the Experimental Model was made on the basis of the voltage ratings of the best high-frequency, high-power silicon switching transistors which were available at the start of this contract. As mentioned previously, the power transistors of this converter must withstand a voltage of approximately twice the input voltage. For

a 56-volt input level, high-frequency power transistors with breakdown-voltage ratings in excess of 200 volts are needed. These have recently been make available. For example, the new Texas Instrument 2N3846 - 2N3849 transistors appear to be well suited for this application.

It is suggested that future versions of this energy-storage-transformer converter be designed for a 56-volt input level. This should result in an increase in overall efficiency of at least 1%.

VI. CONCLUSIONS

The two primary objectives of this research and development contract were (1) to investigate the application of certain unconventional circuit techniques involving energy-storage transformers to a high-power, high-voltage converter for use with ion engines, and (2) using these techniques to design and construct an Experimental Model of an efficient, rugged, and lightweight converter. A modular approach involving six identical building-block converter stages was used in the design of the 2000-volt, 1600-watt, nondissipatively regulated Experimental Model.

As a result of this work it can be concluded that the use of this type of converter, especially in a modular system, is an excellent approach to employ in meeting certain of the power-conditioning requirements of ion engines. The Experimental Model which was built and tested under this contract exhibits a full-load efficiency of 86.5% and a maximum overall efficiency of 88.8%. The total component weight of the 1600-watt Experimental Model is 16.4 pounds. The general ruggedness and the protection characteristics of the Experimental Model are particularly desirable features. An analytical prediction that, because of the characteristics of the energy-storage transformers, load short circuits would not cause current or voltage surges that would affect any of the converter semiconductors has been verified experimentally.

Based primarily on tests and measurements made on the Experimental Model, certain suggestions for improvements to the design of this type of converter are made in Section V of this report. In particular, it is noted that the available flux swing of the energy-storage transformers could be more fully utilized without serious penalties. As discussed in Section V, it is estimated that an overall component weight reduction of approximately 18.5% would result from this modification and that the efficiency would only be decreased approximately 0.4%. The second most significant suggestion for improvement is the use of a higher input voltage. As discussed in Section V, new high-voltage, high-speed power transistors have recently been made available which appear to be well suited to a converter using the circuit techniques developed under this contract and designed for a 56-volt rather than a 28-volt input level. The use of a 56-volt input voltage should make possible an increase in overall efficiency of at least 1%.

One advantage of the modular concept used in this program of effort is the ease with which the basic converter design can be scaled up and down in voltage and power level and thereby adapted to a wide variety of power-conditioning requirements. For example, the present Experimental Model is designed to provide an output of 2,000 volts and 1,600 watts. By simply adding three more building-block stages identical to the six now being used, an output of 3,000 volts and 2,400 watts could just as easily be provided. A wide variety of series and parallel interconnections of the basic building-block stages is possible with little or no redesign or modification being

necessary. This flexibility of interconnection is greatly facilitated by the fact that, rather than having regulated and unregulated stages, the building-block stages of this converter are all truly identical; the output voltage of each is nondissipatively controlled from a single flip-flop circuit which is common to all stages.

An important potential advantage of a modular system in which all stages are identical is that a degree of redundancy may conveniently be designed into such a system. Each of the building-block stages of the system can be designed to have sufficient reserve power-handling capability and range of output-voltage control such that, if any one stage should fail during the operation of the converter, the remaining stages would be able to provide the full rated output voltage and power of the converter. In order to realize this potential redundancy advantage in the modular system developed under this contract, the overall converter protection circuit used in the Experimental Model would have to be supplemented by a per-stage protection system which would prevent a malfunctioning individual stage from overloading the source. As mentioned in Section V, some preliminary work on a suitable per-stage protection technique was done under this contract, although such redundancy was not a contract requirement or a major objective. This task was not carried to completion. However, this potential redundancy advantage is inherent in the identical-stage modular concept and should certainly be exploited. Completion of the design of a suitable per-stage protection system should be a very minor problem.

Through the use of a 56-volt input level and by making the minor design modifications suggested in Section V, it is felt that modular energy-storage-transformer converters for ion engines and other high-power applications could be built for a wide range of output voltage and power levels to provide an overall conversion efficiency of 87% at a component weight of 8 pounds per kilowatt. This weight per kilowatt figure assumes the desirability of designing individual building-block stages so that they will have a margin of capability which, in the event one stage fails, is adequate to allow the remaining stages to provide full rated output.

Although work under this contract involved the development of a converter to provide a high-voltage output, the basic energy-storage-transformer approach is well suited to a wide range of requirements involving low-voltage as well as high-voltage outputs. Multiple outputs at different dc levels can also be provided. Because the characteristics of this converter are inherently different from those of more conventional converters, there may be various special applications to which this type of converter is exceptionally well suited. One major difference between this type of converter and conventional types is that in this converter the secondary windings of the power transformers, i.e. the energy-storage transformers, actually appear as current sources rather than voltage sources. This fact has been used to good advantage in designing the protection system of the converter developed under this contract. It could also be used to excellent advantage, for example, in the application of these general circuit techniques to a converter for cyclically charging a bank of energy-storage capacitors.

One application requiring an efficient, lightweight converter for cyclically charging relatively large energy-storage capacitors is the pulsed-coaxial-accelerator class of electric thrustors. The basic techniques discussed in this report should be exceptionally well suited to this application; the "output filter capacitor" of the converter would simply be the energy-storage capacitor of the coaxial accelerator. For reasons previously explained, the energy-storage capacitors would cause no current transients through any other components of the converter. Because the power transformers would inherently function as nondissipatively controllable current sources, such a converter should not only be very efficient but should also be physically very simple as well. For the same basic reasons which are discussed in this report in relation to the voltage-regulated converter developed under this contract, a modular configuration would also seem to have definite merits for a capacitor-charging application such as the coaxial accelerator.

APPENDIX A. PARTS LIST FOR EXPERIMENTAL MODEL

BUILDING-BLOCK CONVERTER STAGE (SIX USED)

ITEM	DESCRIPTION
Q1, Q2	TRANSISTOR, MHT8302, HONEYWELL (NOW SOLITRON)
Q3, Q4	TRANSISTOR, 2N2297, FAIRCHILD
D1, D2, D3, D4	DIODE PAIRS, EACH DIODE IN THE CIRCUIT DIAGRAM IS A PARALLEL PAIR, UTR-62, UNITRODE
D5, D6	ZENER DIODE, 1N2991B, MOTOROLA
D7, D8, D10, D11	DIODE, 1N645, TEXAS INSTRUMENTS
D9	DIODE, 1N3961, GENERAL ELECTRIC
D12	ZENER DIODE, 1N3795B, MOTOROLA
D13	ZENER DIODE, 1N975B, MOTOROLA
R1	RESISTOR, 180 OHM, 1 WATT, IRC TYPE GBT-1
R2, R3	RESISTORS, 470 OHM, 1 WATT, IRC TYPE GBT-1
R4, R5	RESISTORS, 470 OHM, 1/2 WATT, IRC TYPE GBT-1/2
R6	RESISTOR, 0.33 OHM, 2 WATT, IRC TYPE AS2
C1	CAPACITOR, 3.2 MFD., 35 VDC, TEXAS INST. SCM-2
C2, C3	CAPACITORS, 22 MFD., 400 VDC, SPRAGUE TYPE 202D226X0400D3
T1, T2, T3, T4	SEE APPENDIX B

FLIP-FLOP (ONE USED)

ITEM	DESCRIPTION
Q5, Q6	TRANSISTORS, 2N1132, TEXAS INSTRUMENTS
Q7, Q8	TRANSISTORS, 2N2909, GENERAL ELECTRIC
D14, D15, D16, D17	DIODES, 1N916, GENERAL ELECTRIC
R7, R8, R25	RESISTORS, 1,000 OHMS, 1 WATT, IRC TYPE GBT-1
R9, R10, R15, R16	RESISTORS, 470 OHMS, 1/2 WATT, IRC TYPE GBT-1/2
R11, R12, R13, R14	RESISTORS, 2,200 OHMS, 1/2 WATT, IRC TYPE GBT-1/2
R23, R24	RESISTORS, 4,700 OHMS, 1/2 WATT, IRC TYPE GBT-1/2
R19, R20	RESISTORS, 470 OHMS, 1 WATT, IRC TYPE GBT-1
R17, R18, R21, R22	RESISTORS, 100 OHMS, 1/2 WATT, IRC TYPE GBT-1/2
C4, C5, C6, C7	CAPACITORS, 68 PICOFARADS, 1000 V, SILVER MICA, ARCO-ELMENCO
C8, C9	CAPACITORS, 22 MFD, 70 VDC, SPRAGUE TYPE 130D
C10, C11	CAPACITORS, .001 MFD, 100 V, SPRAGUE 191P1020152

INPUT FILTER (ONE USED)

ITEM	DESCRIPTION
C_C	3 PARALLEL CAPACITORS, EACH 5000 MFD, 50 VDC SPRAGUE TYPE 36D
L_C	SEE APPENDIX B

APPENDIX A. (CONT.)

REGULATION AND PROTECTION CIRCUIT (ONE USED)

ITEM	DESCRIPTION
UJT1	UNIJUNCTION TRANSISTOR, 2N491A, GENERAL ELECTRIC
Q9, Q14	TRANSISTORS, 2N1132, TEXAS INSTRUMENTS, FAIRCHILD
Q10, Q11, Q12	TRANSISTORS, 2N2909, GENERAL ELECTRIC
Q13	DUAL TRANSISTOR, 2N2640, TEXAS INSTRUMENTS
D18	ZENER DIODE, 1N963B, MOTOROLA
D19, D20, D22, D24, D25	DIODES, 1N645 TEXAS INSTRUMENTS
D21	ZENER DIODE, 1N967B, MOTOROLA
D23	ZENER DIODE, 1N941B, MOTOROLA
S1	SWITCH, SPST, CUTLER-HAMMER TYPE 8866K7
R26, R34	RESISTORS, 1,500 OHMS, 1/2 WATT, IRC GBT-1/2
R27, R41	RESISTORS, 330 OHMS, 1/2 WATT, IRC GBT-1/2
R28, R29, R44, R45	RESISTORS, 4,700 OHMS, 1/2 WATT, IRC GBT-1/2
R30, R40, R48	RESISTORS, 1,000 OHMS, 1/2 WATT, IRC GBT-1/2
R31	POTENTIOMETER, 15,000 OHMS, 1 WATT
R32	RESISTOR, 1,000 OHMS, 1 WATT, IRC GBT-1
R33	RESISTOR, 7.5 OHMS, 10 WATTS, DALE RH-10
R35	POTENTIOMETER, 50 000 OHMS, 1/2 WATT
R36	RESISTOR, 2,200 OHMS, 1/2 WATT, IRC GBT-1/2
R37	RESISTOR, 6,800 OHMS, 1/2 WATT, IRC GBT-1/2
R38	RESISTOR, 2,700 OHMS, 1/2 WATT, IRC GBT-1/2
R39	RESISTOR, 1,680 OHMS, 1/2 WATT, IRC GBT-1/2
R42	RESISTOR, 976 KILOHMS, 1%, IRC TYPE MEC (actually comprised of ten 97.6 K, 1-watt resistors in series)
R43	RESISTOR, 5.58 KILOHMS, 1/2 WATT, 1% (actually comprised of 7.32 K in parallel with a series combination of 22 K and 1.5 K)
R46	RESISTOR, 270 OHMS, 1/2 WATT, IRC GBT-1/2
R47	RESISTOR, 470 OHMS, 1/2 WATT, IRC GBT-1/2
R49	RESISTOR, 10 OHMS, 1 WATT, IRC GBT-1
C12, C14, C20, C22	CAPACITORS, 22 MFD, 70 VDC, SPRAGUE 130D
C13	CAPACITOR, 2.2 MFD, 35 VDC, ASTRON TES
C15	CAPACITOR, 1.0 MFD, 15 VDC, SPRAGUE 150D
C16, C19	CAPACITORS, 0.005 MFD, 400 V, SPRAGUE
C17	CAPACITOR, 110 MFD, 6 V, NONPOLARIZED SPRAGUE 151D
C18, C21	CAPACITORS, 0.047 MFD, 35 VDC, TEXAS INSTRUMENTS SCM-2
L1	INDUCTOR, 1250 MICROHENRY, DELEVAN 492416

APPENDIX B. DESCRIPTION OF MAGNETIC ELEMENTS

T1, T2 - - - ENERGY-STORAGE TRANSFORMERS

Core: Arnold Engineering Company No. AM2549
(Cut C core, 1-mil grain-oriented silicon-iron material)

Air Gap: 0.014 inch total; 0.007 inch on each side of C core

Windings:
N1: 26 turns, 2 strands #16 Heavy Polythermaleze
N2, N3: 195 turns, #26 Heavy Polythermaleze

T3, T4 - - - SATURABLE CURRENT TRANSFORMERS

Core: Magnetics, Inc. No. 52086-1D
(Tape wound core, 1-mil Square Permalloy 80)

Windings:
N1: 100 turns, #30 Heavy Formvar
N2: 20 turns, #20 Heavy Polythermaleze
N3: 2 turns, 2 strands #16 Heavy Polythermaleze

L_o - - - INPUT FILTER CHOKE

Core: Arnold Engineering Company No. AM2549
(Cut C core, 1-mil grain-oriented silicon-iron material)

Air Gap: 0.014 inch total; 0.007 inch on each side of C core

Winding: 4 turns, 35 strands #20 Heavy Formvar

APPENDIX C. COMPARISON OF ELECTRICAL STRESSES AT FULL LOAD TO COMPONENT RATINGS FOR MAIN POWER-HANDLING COMPONENTS

COMPONENT	RATING	ACTUAL STRESS	SAFETY FACTOR
Transistors Q1, Q2 (Honeywell MHT8302)	I_c(max) = 30 a	13 a (peak) 5.5 a (average)	5.5
	BV_{CBO} = 100 v	84 v (1-usec clipped spike)	1.2
		60 v (sustained while off)	1.7
	BV_{EBO} = 8 v	4.2 v	1.9
	Power Diss. = 100 w at 100°C case temp.	4.6 w	22
Rectifiers D1-D4 (Unitrode UTR-62 in parallel pairs)	$I_{avg.}$ = 1.2 a @ 100°C (per single device)	0.4 a (per parallel pair)	3-6 (depending on current sharing)
	PIV = 600 v	340 v (sustained while blocking)	1.8
		1020 v (transient, see Section IV)	None
Zener diodes D5, D6 (Motorola 1N2991B)	Power Diss. = 10 w	1.3 w	7.7

NOTE:

The electrical stresses during the transient interval following the firing of a thyratron across the load or following the application of a direct short circuit with a metallic conductor were found not to exceed the above full-load stresses. Reasons for this are discussed in Section III of this report.